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SINGLE DC-SOURCE-BASED SEVEN-LEVEL BOOST-INVERTERFOR ELECTRIC VEHICLE APPLICATIONS

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ABSTRACT
This research presents a circuit layout for a multilevel inverter that can enhance the number of output voltage levels while using fewer devices. This study proposes a single dc- source-based seven-level inverter (LI) with boosting capacity. To provide seven-level boosted output, the suggested inverter uses eight switches, two diodes, two capacitors, one inductor, and a single dc source. The suggested inverter is suited for electric vehicles because it uses a single dc supply and has boosting capabilities, requiring less series-connected battery cells. The proposed 7LI uses phase-shifted pulse-width modulation (PWM), a multi-carrier-based PWM technology, to generate switching pulses. A device count-based comparison of the proposed inverter to recent topologies is carried out**.** Simulation is used to assess the viability and impact of the proposed inverter, which is then validated with a laboratory prototype.

INTRODUCTION
The electric motor is driven by an inverter, which is built to the exact specifications of the EV traction drive. In the case of bigger EVs like buses and trucks, where modular inverter design is more practical, a high-power inverter is required. The traditional two- level voltage-source inverter (VSI) for drive has two major drawbacks: I in electric vehicles, the development of high- frequency ripple current at the dc bus, which increases as the ambient temperature rises. As a result, a larger capacitor is required, lowering the EV's power density and efficiency. (ii) In order to commutate large motor currents, VSI is run at a higher switching frequency, which results in substantial switching losses. Multilevel inverters (MLIs) have less filter requirements, lower electromagnetic interference, lower switching losses, and less stress on switches than two-level inverters (LIs). To overcome the limits of the 2LI and to take into account the needs of electric vehicles, the MLI is a better power converter.
In order to increase the number of output levels while reducing the number of devices, the number of voltage sources must also rise. Several MLI topologies using a single dc source are presented in to address this issue. proposes a 7LI with seven switches, two diodes, and three capacitors that operates with a single dc supply. proposes a 5LI based on packed U-cells. Six switches, one capacitor, and a dc source make up this circuit.
For a seven-level operation, MLI in requires a series–parallel connection of three capacitors and one dc voltage source. Sun et al. present 7LI, a single dc-source based on switching capacitors. proposes a switched-capacitor-based 9LI for high- frequency applications. Because the availability of dc sources in the form of batteries is restricted, these topologies are appealing for EV applications. However, because these battery sources have low voltage ratings, an additional boosting stage following the battery stage will increase EV performance.
MLIs with voltage boosting capability have recently been presented. The boosting stage will minimize the number of batteries required even more. As a result, for an EV application, a single dc-source-operated MLI with boosting capacity is an appropriate solution. Lee et al. present a series of boost switched capacitors for floating capacitors based on 7LIs with self-voltage balancing. presents a switched-capacitor-based 9LI with a maximum boosting capability of twice the input dc source. For photovoltaic applications, Vahedi et al. suggest a modified packed U-cell 7LI. proposes a step-up MLI with fewer switches, however the number of diodes used is large. All of the boost MLIs shown in need a large number of components. The number of devices must be lowered even more.

PROPOSED SYSTEM CONFIGURATION

Figure 1 depicts the suggested inverter. It has three stages:
single-input–dual-output dc–dc (DODC) boost conversion stage,
diode-bypassed switch–dc-source stage, and polarity generation stage [full-bridge converter (FBC)].
The diode-bypassed switch-dc-source converter (DBSDSC) in the second stage receives a boosted dc dual output from a single- input–DODC converter in the first stage. The DBSDSC generates a unipolar staircase waveform which is then converted bipolar by connecting the FBC in series at the end. The FBC is used to link the load. Capacitors C1 and C2 are charged to voltages V1 and V2, respectively, and serve as inputs to the DBSDSC in Figure 1. The DBSDSC's asymmetric input dc (V1 V2) operation produces more output voltage levels than the symmetric input dc (V1 = V2) operation. DBSDSC with asymmetric input mode will run DODC generating boosted output at two distinct voltage levels, resulting in a need. The next sections go over the specific operationsof DODC and DBSDSC.
For the same amount of dc sources, a DODC converter has more output levels.

The benefits of including DODC are as follows:

- Because of the multi-output feature, fewer dc sources are required.
- Asymmetric dc sources can be made from symmetrical dc sources.
- Because of the increased voltage created by the low input voltage, fewer battery cells arerequired.
- The number of devices has been reduced.

DODC converts a single dc source from EV batteries into two separate dc voltage levels and offers asymmetrical dc input for DBSDSC operating the electric motor's seven-level operations. The inclusion of DODC minimizes the need for batteries, resulting in a smaller and less expensive battery bank in an EV. DODC also generates asymmetrical input for DBSDSC, resulting in larger output voltage levels and hence lowering the *filter.*

DODC CONVERTER

Figure 2 shows the circuit diagram for the dual-output boost converter. Two switchesS_a, S_b two diodes D1, D2, two capacitors C1, C2, and an inductor L make up this circuit.
As illustrated in Fig. 3, DODC functions in three different modes. The inductor is charged in the first mode, which involves turning on switch Sa and turning off switch S_b. The inductor current travels through switch $S_a$and diode D1 to charge capacitor C1 in the second mode, with switch Sb on and switch S_a off.
Both switches S_a and S_b are turned off in the third mode, and inductor current flows through diode D2 to charge both capacitors C1 and C2.

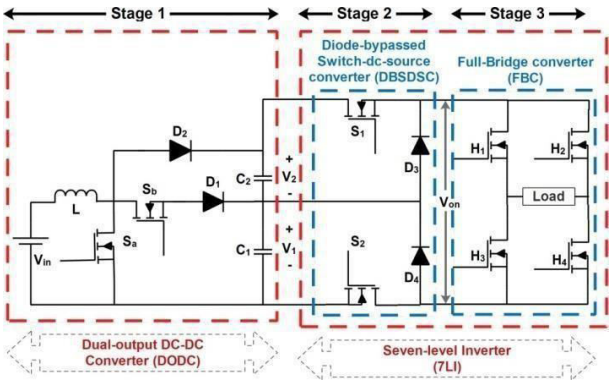


FIGURE-1: PROPOSED CONVERTER

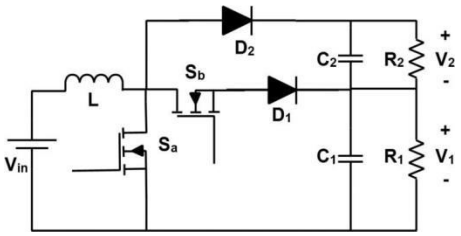


FIGURE 2: DODC

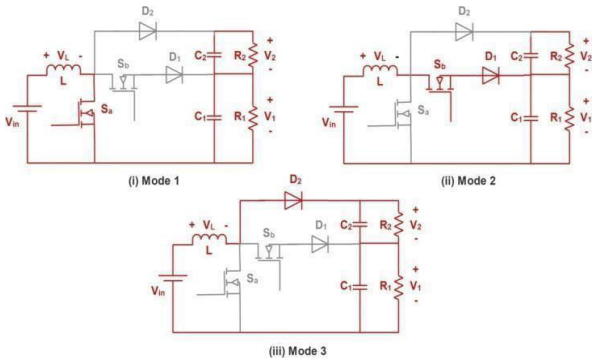
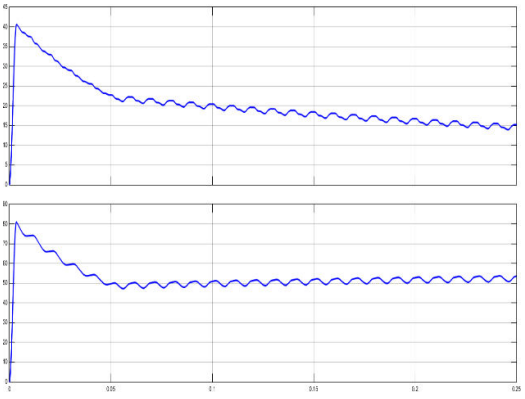


FIGURE 3: STAGE 1 MODES OF OPERATION

MODES	SWITCH(Sa)	SWITCH(Sb)	C1	C2
1	On	Off	Discharging	discharging
2	Off	On	Charging	discharging
3	Off	Off	Charging	charging

TABLE-1: Charging states during modes of operation

Table 1 summarizes the charging states of capacitors C1 and C2 during three modes of operation. The voltage available across the capacitors C1 and C2 is determined by the duty ratios of switches Sa and Sb.



The waveform obtained at stage-1

DIODE BYPASSED SDSC

In Figure 4, a diode-bypassed SDSC DBSDSC in series with an FBC operates as 7LI, with a total of six switches and two diodes operating with asymmetric input voltages. The diode is present to bypass the switch and dc source being linked in series. It has eight different modes of operation. Switching states are summarized in Table 2.

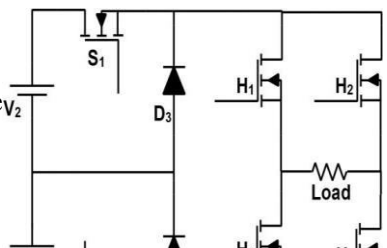


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FIGURE-4: 7LI

LEVEL	VOLTAGEOUTPUT (V0)	CONDUCTINGDEVICE
1	V1	S2, H1, H4, D3
2	V2	S1, D4, H1, H4
3	V1 + V2	S1, H1, H4, S2
4	0	D3, D4, H1, H4
5	-V1	D3, D4, H1, H4
6	-V2	S1, D4, H2, H3
7	-(V 1+V2)	S1, D4, H2, H3
8	0	D1, D2, H2, H3

TABLE-2: SWITCHING STATES OF DEVICE IN 7LEVEL INVERTER

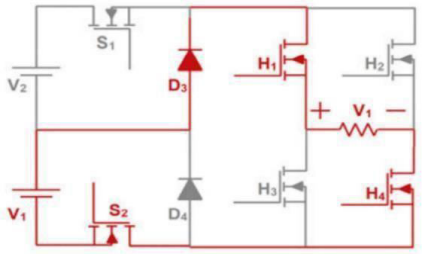

FIGURE: 5a

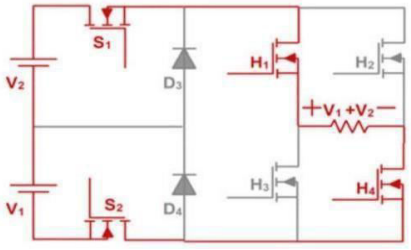

FIGURE: 5b

In mode 1, V2 is bypassed through diode D3 while turning off the switch S1 and turning on theswitch S2, making voltage V1 appear across the load. (fig: 5a)

In mode 2, the voltage V1 is bypassed through diode D4 while switching off switch S2 and onswitch S1, resulting in V2 across the load.

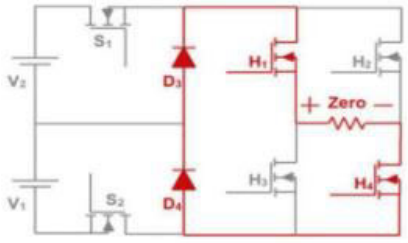

FIGURE: 5c

By turning on both S1 and S2, both voltage sources V1 and V2 are connected in series in mode 3 and V1 + V2 appears across the load. Both voltage sources V1 and V2 are bypassed in mode 4, resulting in zero voltage across the load.

Switches H1 and H4 of the FBC conduct from mode 1 to mode 4, resulting in a positive half of the staircase waveform at the load, as shown in Fig. 5. Modes 5–8 are a repeat of modes 1–4, with the exception that the conductions of H2 and H3 of the FBC are changed, resulting in the negative half of the staircase waveform at the load. After four modes (Fig:5(a-d)) of operation, the **staircase waveform** with seven levels depicted in Fig. 6 is obtained at the load. The addition of two dc sources as V1 + V2 generates the maximum number of output voltage levels created by the 7LI, as shown in Table 2. As a result, the 7LI generates a higher voltage amplitude. As a result, the 7LI can only generate seven equal voltage levels at the output if the second dc source (V2) has twice the amplitude of the first one (V1). It implies that when V2 = 2V1, the output staircase waveform contains the following levels: 0, V1, 2V1, and 3V1. The proposed inverter's voltage sources V1 and V2 are the output voltages of DODC acquired across capacitors C1 and C2, as illustrated in Fig. 1. To obtain the output of DODC as V1 and V2=2V1, it follows that, $d0$ as 0.6 and $d1$ as 0.2.

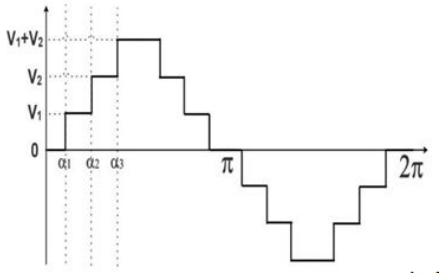

FIGURE. 6 SEVEN LEVEL STAIRCASE WAVEFORM

The whole process of analyzation is worked with these values.fig-7 shows the inverter whichcan be connected and used for 3-phase applications.

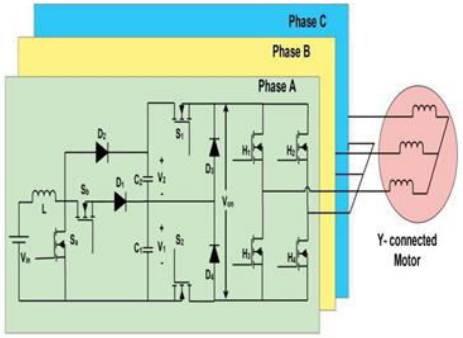

FIGURE. 7 THREE PHASE ARRANGEMENT OF THE PROPOSED INVERTER

MODULATION STRATERGY

Different modulation approaches are available in the literature to generate a staircase waveform in MLIs. To generate gate pulses for the switches in the suggested inverter, phase-shifted pulse- width modulation (PSPWM) is used in this article. A single reference is compared with a (n 1) carrier signal that is phase shifted by ((n 1)/2) degrees in PSPWM, where n is the number of output levels in MLI.

To get these signals the circuit is been connected as shown in figure-8 for the simulation.

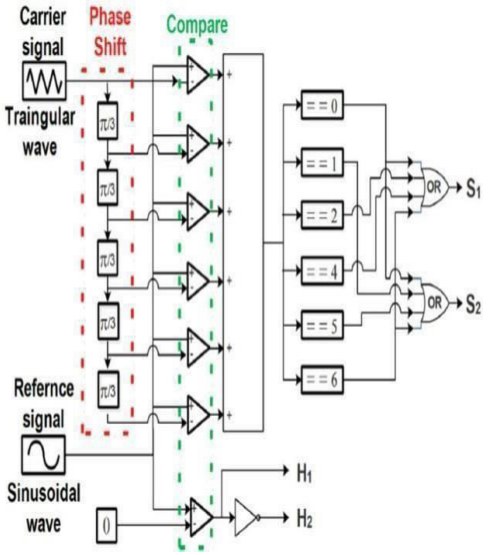

FIGURE8: LOGIC CIRCUIT OF PSPWM FOR 7 LEVEL- MLI

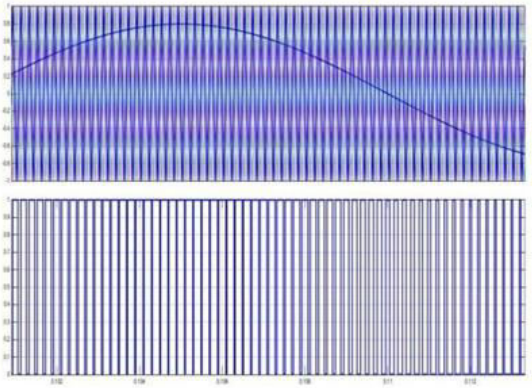

FIGURE 9: REFERENCE AND CARRIER GATE SIGNAL

As shown in Fig. 9a, the proposed 7LI compares a reference signal (sine wave) with six carrier signals (triangular waves) shifted by (2π/6) degrees. Figure 9b depicts the PSPWM modulation logic. The modulation index M is defined as the ratio of the peak of the reference sinusoidal signal to the peak of the carrier triangle wave in this modulation technique.

COMPONENTS	**VALUES**
Mosfet	200 V, 12 A
Diode	650 V, 10 A
Capacitor	100 V, 330 µF
Inductor	560 µH, 7 A
Resistive	90 Ω
Resistive-inductive load	R = 90 Ω, L = 25mH
LC output filter	L = 560 µH, C = 10µF
Inverter switching frequency	5 kHz

TABLE-3 : CIRCUIT PARAMETERS FOR SIMULATION

SIMULATION RESULTS

Simulation studies of the suggested inverter are performed using MATLAB/Simulink to study the performance analysis of the proposed inverter. The input dc voltage is maintained at 24 V, the inverter is switched at a frequency of 5 kHz, and the output is created at 50 Hz.The above table lists out the parameters used for the circuit to perform simulation.

V1 = Vin = 24 V and V2 = 2Vin = 48 V are obtained using the DODC converter depicted in Fig. 2 with d0 = 0.6 and d1 = 0.2. As a result, the 7LI in Figure 4 will work with asymmetric input.

V1 and V2 are dc voltages that generate a seven-level output. To give gate pulses to the switches S1 and S2, the PSPWM switching technique depicted in Fig. 8 is used. PSPWM has a switching frequency of 5 kHz and a modulation index (M) of 0.8. The H-bridge switches convert the unipolar staircase voltage Von generated by the DBSDSC into the necessary bipolar seven-level output at a fundamental output frequency of 50 Hz. The proposed three-phase inverter is simulated for R load (R = 90) and RL load (R = 90 and L = 25 mH) in Fig. 8. To get the desired output the LC-Filter is been placed at the load side as presented in figure 10.

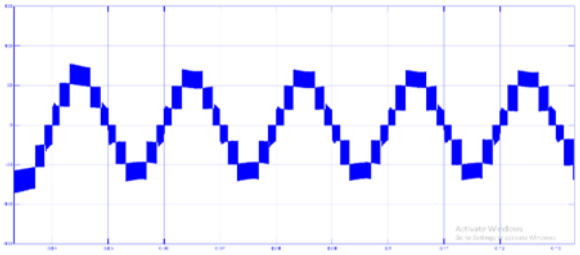

FIGURE-10:7-LEVEL STEPPED STAIRCASE WAVEFORM

The below figures shows the voltage and current wave forms with and without filter for R-LOAD and R-L load

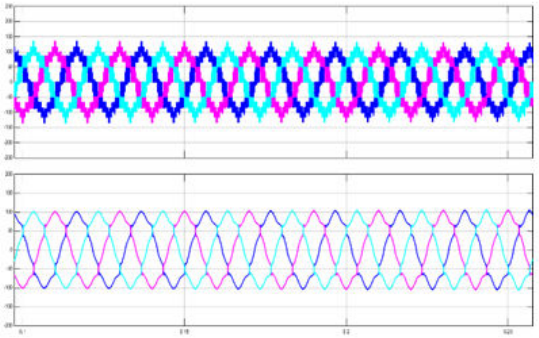

FIGURE.11: VOLTAGE WAVEFORM FORRLOAD

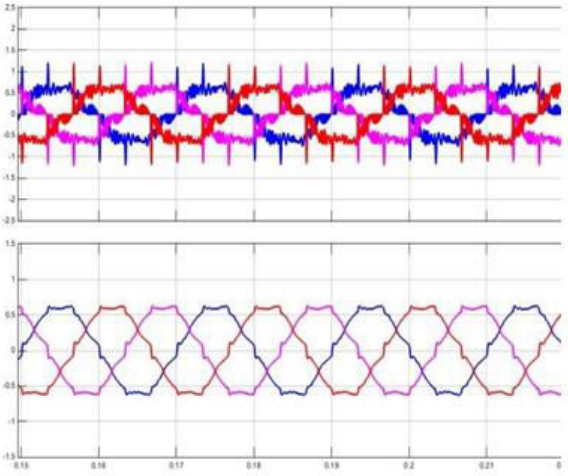

FIGURE-12: CURRENT WAVEFORM - R-LOAD

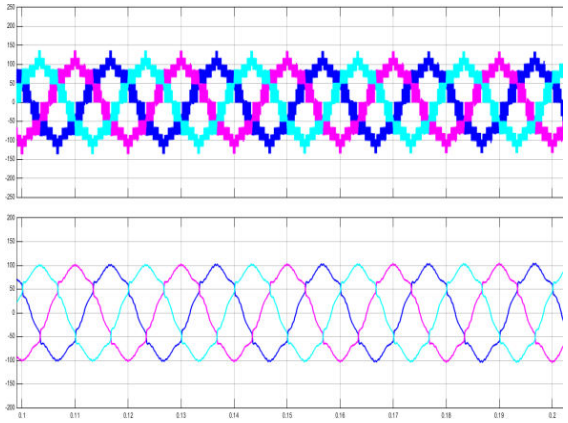

FIGURE 13: VOLTAGE WAVEFORM R. L LOAD

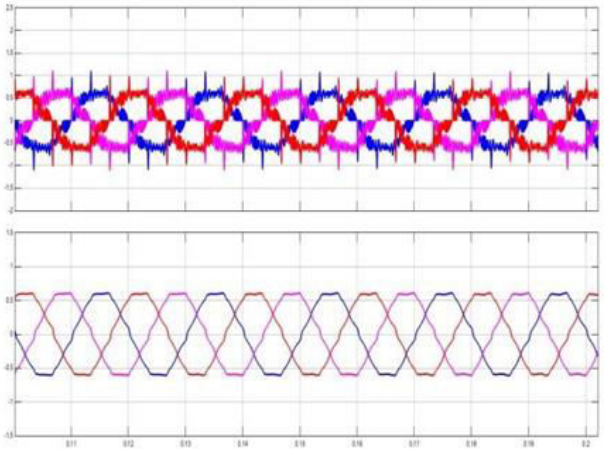

FIGURE 14: CURRENT WAVEFORM FOR R.L-LOAD

FFT AND THD ANALYSIS OF CASCADED H-BRIDGESEVEN-LEVEL MLI:

Figure . 15 AND 16 depicts the variance in output total harmonic distortion (THD) for various values of the modulation index M. With d0 = 0.6 and d1 = 0.2, the output THD is simulated for a resistive load (R = 90). THD varies from 28.66 to 6.79 percent when the modulation index is changed from M = 0.5 to 1. M = 0.55 has a maximum THD of 28.66percent. whereas M = 1 has a minimum THD of 6.79 percent. The change of ac voltage gain obtained in the proposed inverter is shown in Fig. 13. The ratio of the output root-mean-square (RMS) voltage (Vrms) to the dc input voltage is known as voltage gain in output ac (Vin). The ac voltage gains for the proposed inverter operating with input dc voltage Vin = 24 V, d0 = 0.6, and M = 0.5 to 1 is plotted using simulation results for a variation in modulation index M

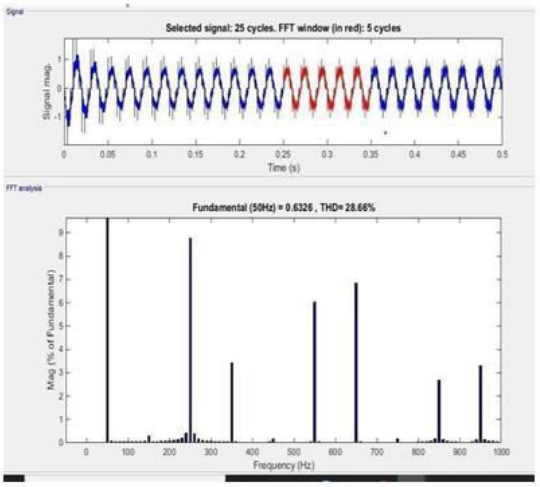

FIGURE-15: THD IN DISCRETE FORMWITHOUT FILTER

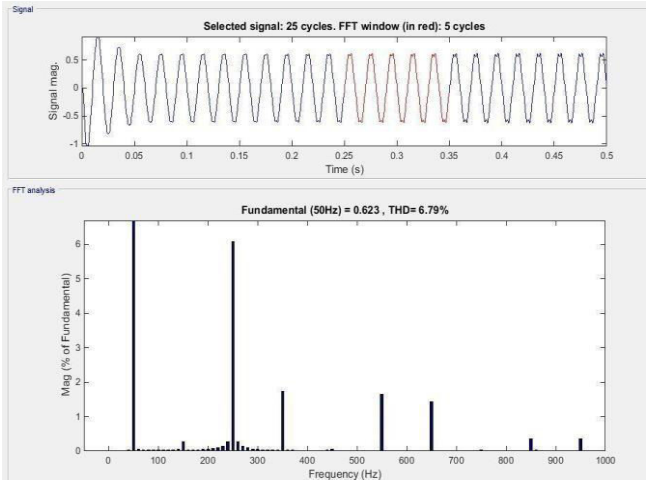

FIGURE-16: THD IN DISCRETE FORM WITH FILTER

CONCLUSION

By cascading a single-input–DODC, DBSDSC, and FBC–this work presents a single dc-source seven-level boost inverter. The asymmetric operation of 7LI is facilitated by the operation of DODC for producing two voltages at different voltage levels, resulting in a higher number of levels for the same device count. The suggested inverter's single-dc-source operation and boosting function decrease the need for battery cells as dc sources for inverter operation in EVs. In comparison to existing single dc-source multilevel topologies and boosted multilevel topologies, the proposed inverter requires less device counts and input dc sources for seven-level output. Four switches in the H-bridge network of the proposed inverter operate at the fundamental output frequency, while the remaining four switches function at the higher switching frequency. The voltage stress in H-bridge switches, on the other hand, is higher than in the other four switches. DODC is used in the proposed work with d0 = 0.6 and d1 = 0.2 to create two separate voltage levels Vin and 2V2.

This operating state was chosen in order to generate seven levels with the least amount of THD. To validate the proposed inverter's performance, a hardware prototype of a three-phase proposed inverter is created. For M = 0.8, boosted ac voltage with 1.67 ac gain is produced. At M = 1, d0 = 0.6, and d1 = 0.2, the suggested inverter may achieve a maximum ac gain of 2.1 times. For different values of d0 and d1, output ac gains greater than 2.1 is also achievable.

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