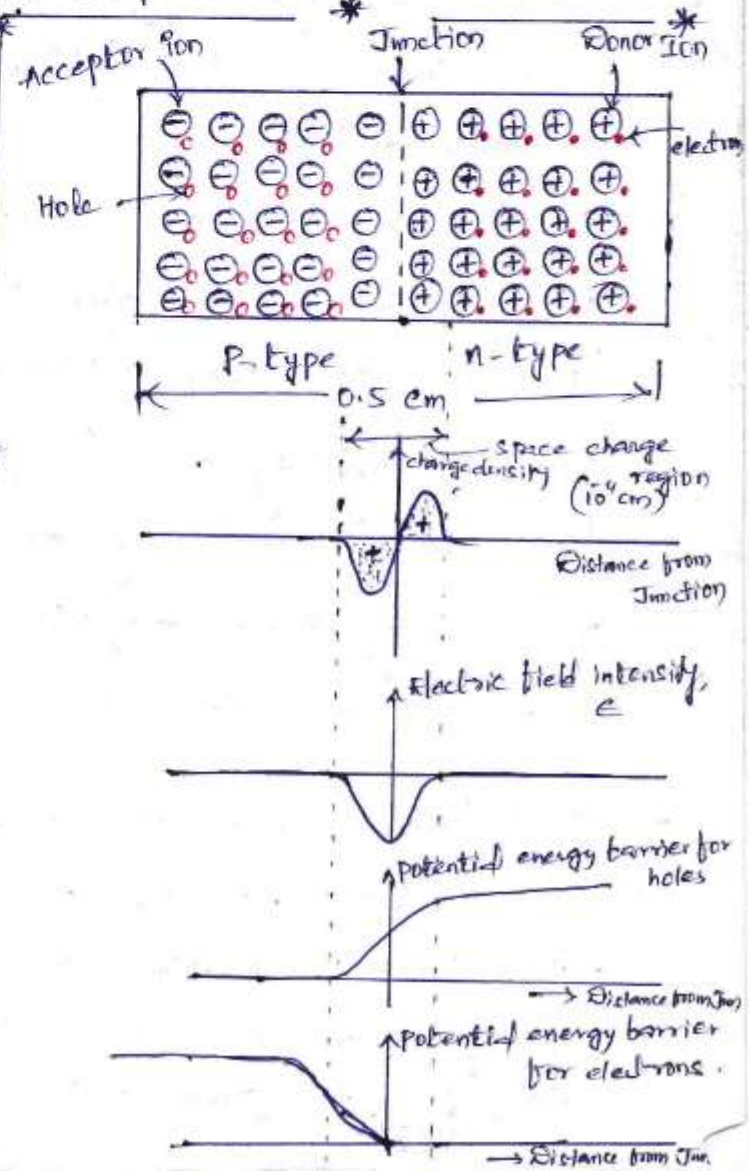
Qualitative Theory of the P-N Junction:—

If donor impurities are introduced into one side and acceptors into the other side of a single crystal of a semiconductor, a p-n junction is formed. The donor ion is indicated by a plus sign because after this impurity atom donates an electron, it becomes a positive ion. The Acceptor ion is indicated by a minus sign because after this atom accepts an electron, it becomes a negative ion. Initially, there are p-type carriers to the left of the junction and only n-type carriers to the right. Because there is a density gradient across the junction, holes will diffuse to the right across the junction and electrons to the left.

As a result of the displacement of these charges, an electric field will appear across the junction. Equilibrium will be established when the field becomes large enough to restrain the process of diffusion.

The electric charges are confined to the neighborhood of the junction, and consists of immobile ions. The positive holes which neutralized the acceptor ions near the junction in the p-type germanium have disappeared as a result of combination with electrons which have diffused across the junction. Similarly, the neutralizing electrons in the n-type Ge have combined with holes which have crossed the junction from the p material.

→ The unneutralized ions in the neighborhood of the junction are referred to as 'uncovered charges'.



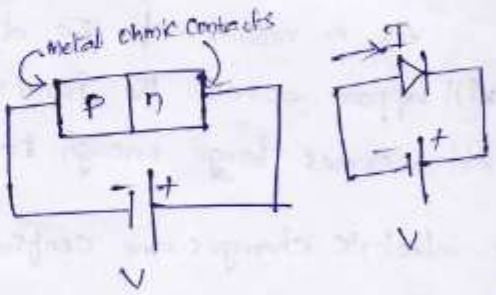
Since the region of the junction is depleted of mobile charges, it is called the "depletion region", the 'space charge region' or the 'transition region'. The thickness of this region is of the order of $10^{-4}cm = 10^{-6}m = 1$ micron.

→ There is a variation in Electrostatic potential in the depletion region. This variation constitutes a potential energy barrier against the flow of electrons from the n-side across the junction or flow of holes from the p-side across the barrier.

→ under open circuited conditions the net hole current must be zero.

P-N Junction as a Diode:—

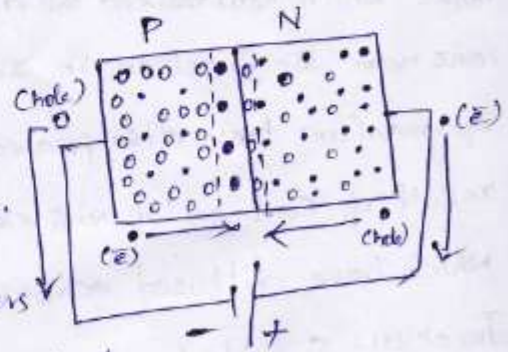
→ The p-N Junction diode permits the easy flow of current in one direction but restrains the flow in the opposite direction.



Reverse Bias:

A battery is connected across the terminals of a p-n junction is called a 'Biasing'.

→ If the negative terminal of the battery is connected to the p-side of the junction, and the positive terminal to the n-side that is called "Reverse Biasing".



→ Since the majority carriers in p-side are holes and minority carriers are electrons. The majority carriers and minority carriers in N-side are electrons and holes respectively.

→ The polarity of connection in Reverse Bias is to cause both the holes in the p-type and the electrons in the n-type to move away from the junction. consequently, the region of negative charge density is spread to the left of the junction and the positive charge region spread to the right i.e. the width of the depletion region

depletion region increases. However, this process cannot continue indefinitely, because in order to have a steady flow of holes to the left, these holes must be supplied across the junction from the n-type Germanium es Silicon. And there are very few holes in the n-type side. Hence, nonfinally zero Current Results.

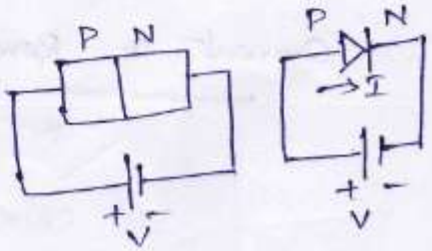
Actually, a small Current does flow because a small number of hole-electron pairs are generated throughout the crystal as a result of thermal energy. The holes so formed in the n-type will wander over to the junction. A similar remark applies to the electrons thermally generated in the p-type. This small Current is the diode "Reverse saturation Current", and its magnitude is designated by I_o. This Reverse Current will increase with increasing temperature and hence the back resistance of a crystal diode decreases with increasing temparature.

→ When the Reverse Bias of V is applied to the diode, the height or width of the potential barrier increased by the amount eV. This increase in the barrier height serves to reduce the flow of majority carriers. However, the minority carriers are uninfluenced by the increased height of the barrier. So in Reverse Bias, Cussent is caused due to minority carriers only. so the Current exist in Reverse Bias is Minority Carrier Current. which is in the order of MA. (Micro-Amperes i.e, in the order of 10^{-6}A).

→ Reverse Bias is also called "Blocking Bias".

forward Bias:—

If P-material is connected to positive polarity of Battery and n-material is connected to negative polarity of Battery. This type of Biasing is called "forward Biasing".



→ for such a diode, the height of the potential barrier at the function will be lowered by the applied forward voltage V.

→ In p-side Majority carriers are holes and minority carriers are electrons and in n-material majority carriers are electrons and minority carriers are holes.

When diode is connected in forward Bias, one to the attractive force minority carriers on either side of the function are attracted by the Battery and Majority carriers are moving away from the Battery and crosses the depletion region due to the repeller force and becomes the minority carriers on other side i.e. holes from crosses the barrier p side to n side and electrons from n-side to p-side and these can cause Current.

Here the Current is Causes due to the majority carriers so this Current is majority carrier Current in forward Bias.

Here Electrons and holes on either side of the function are crossing the barrier from higher concentration region to lower concentration region. so this type of Current is called "Diffusion Current".

The diffusion Current is possible when there is a gradient of concentration levels.

→ In forward bias, Current Causes is due to majority carriers but in Reverse Bias, Current Causes due to minority carriers. so Current in forward Bias is more [in the order of mA] than the Current in Reverse Bias [in the order of μA].

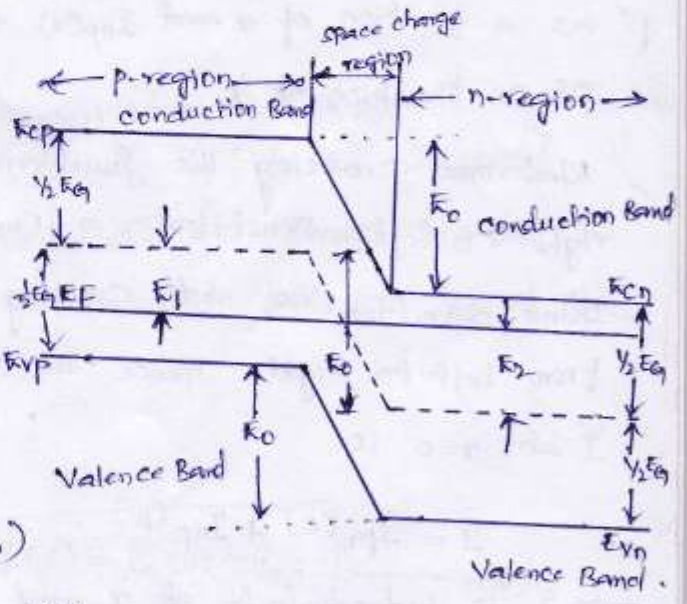
Band structure of an open circuited p-n Junction:—

Generally a p-n junction is formed by placing p- and n- type materials side by side i.e., in intimate contact on an atomic scale. Under these conditions the fermi level must be constant throughout the specimen at equilibrium. If this were not so, electrons on one side of the junction would have an average energy higher than those on the other side, and there would be a transfer of electrons and energy until the fermi levels in the two sides did line up.

→ fermi level is (E_F) closer to the conduction band edge (E_{cn}) in the n-type material and closer to the Valence Band edge (E_{vn}) in the p-side. clearly, the conduction band edge (E_{cp}) in the p-material cannot be at the same level as (E_{cn}), nor can the Valence band edge (E_{vn}) in the n-side line up with (E_{vp}). Hence the energy band diagram for a p-n junction appears as shown in figure, where a shift in energy levels E_0 is indicated.

i.e. $E_0 = E_{cp} - E_{cn} = E_{vp} - E_{vn} = E_1 + E_2$

This energy E_0 represents the potential energy of the electrons at the junction.



from figure, we see that

$$E_F - E_{vp} = \frac{1}{2}E_g - E_1 \longrightarrow (1)$$

and

$$E_{cn} - E_F = \frac{1}{2}E_g - E_2 \longrightarrow (2)$$

from (1) & (2),

$$E_0 = E_1 + E_2 = E_g - (E_{cn} - E_F) - (E_F - E_{vp})$$

$$= E_g + E_{vp} - E_{cn} \longrightarrow (3)$$

Since $np = N_c N_v e^{-(E_c - E_v)/kT} = N_c N_v e^{-E_g/kT} \longrightarrow (4)$

and $np = n_i^2 \longrightarrow (5)$

from (3) & (4), $E_g = kT \ln\left(\frac{N_c N_v}{n_i^2}\right)$

Since we have, $E_F = E_c - kT \ln\left(\frac{N_c}{N_D}\right)$ & $E_F = E_v + kT \ln\left(\frac{N_v}{N_A}\right)$

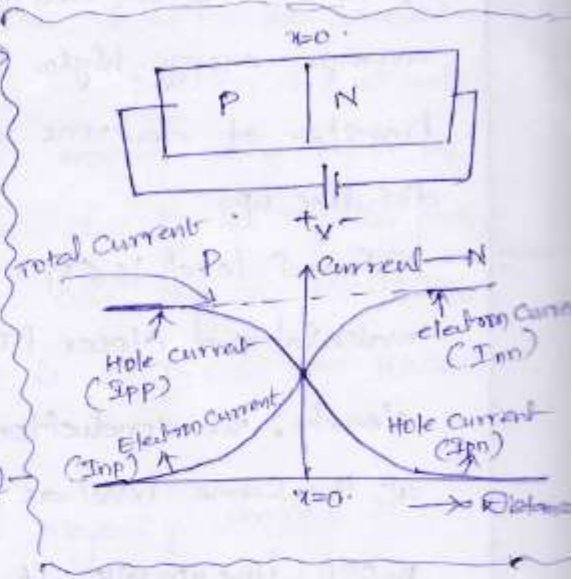
$\therefore E_{cn} - E_F = kT \ln(N_c/N_D) \longrightarrow (6)$ $\quad \therefore E_F - E_{vp} = kT \ln\left(\frac{N_v}{N_A}\right) \longrightarrow (7)$

Substituting from Eqn's (5), (6) and (7) in (4) yields

$$E_0 = KT\left(\ln\frac{N_c N_v}{n_i^2} - \ln\frac{N_c}{N_D} - \ln\frac{N_v}{N_A}\right) = KT\ln\left(\frac{N_c N_v}{n_i^2}\frac{N_D}{N_c}\frac{N_A}{N_v}\right)$$

$$E_0 = KT\ln\left(\frac{N_D N_A}{n_i^2}\right) \quad ev. \quad [ev \rightarrow \text{Electron volts}]$$

Current components in a p-n Diode:



When a forward Bias is applied to a diode, holes are injected into the n-side and electrons into the p-side. The number of these injected minority carriers falls off exponentially with distance from the junction. Since the diffusion current of minority carriers is proportional to the concentration Gradient, this current must also vary exponentially with distance.

There are two minority currents I_{pn} and I_{np}, are represented in figure. $I_{pn}(x)$ represents the ~~electron~~ hole current in the p-side as a function of x and $I_{np}(x)$ represents the electron current in the p-side as a function of x.

Electrons crossing the junction at $x=0$ from right to left constitutes a current in the same direction as holes crossing the junction from left to right. Hence the total current I at $x=0$ is

$$I = I_{pn}(0) + I_{np}(0)$$

I_{pn} → Hole current in n-side
I_{nn} → electron current in n-side
I_{np} → electron current in p-side
I_{pp} → hole current in p-side

$I_{S_1S_2}$

S_1 → current due to type of carriers

S_2 → current in the type of material.

→ I is independent of x and is indicated as a horizontal line. Consequently there must be a second component of current I_{pp}, which when added to I_{np} gives the total current I.

→ The characteristics shown diode is a symmetrically doped diode. so the curves are combined on the $x=0$. for symmetrically doped, $I_{pn} = I_{np}$.

→ If doping concentration is not same, current components cannot merged on $x=0$ line.

→ Generally we can write, $I = I_{pp}(x) + I_{np}(x)$

Diode Current Equation :

→ To derive the expression for the total current as a function of applied voltage. Let us assume that we neglect the depletion layer thickness, and hence Barrier width is zero.

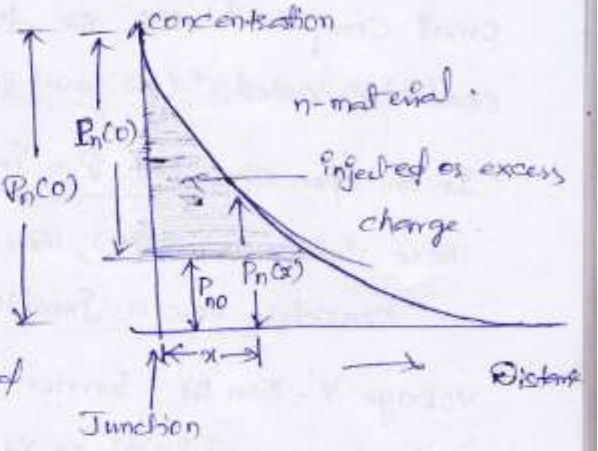
If a forward bias is applied to the diode, holes are injected from the p-side into the n-material. The concentration of [P_n] holes in the n-side is increased above its thermal equilibrium value P_{no} and as indicated in figure.

P_{no} → Hole concentration in n-material under open circuited condition [i.e. without applying any Bias voltage].

$P_n(0)$ → Injected hole concentration in n-material at the junction.

$P_n(0)$ → Total hole concentration in n-material at the junction.

$P_n(x)$ → hole concentration in n-material at x-distance from junction.



from the figure,

$$P_n(x) = P_{no} + P_n(0)\, e^{-x/L_p} \longrightarrow (1)$$

where L_p → diffusion length for holes in the n-material.

Diffusion Length of electrons or holes represents the distance into the semiconductor at which the injected concentration falls to 1/e of its value at x=0.

Since at x=0, from eqn(1)

$$P_n(0) = P_{no} + P_n(0) \Rightarrow \boxed{P_n(0) = P_n(0) - P_{no}} \longrightarrow (2)$$

Since the diffusion hole current in the n-side is given by

$$I_{pn}(x) = -Aq D_p \frac{dP_n(x)}{dx} \longrightarrow (3)$$

[Since $J_p = -q D_p \frac{dP}{dx}$ & $J = \frac{I_p}{A}$ $\therefore I_p = -qAD_p \frac{dP}{dx}$]

Taking the derivative of eqn(1) and Sub in (3), we obtain

$$I_{pn}(x) = \frac{AqD_p P_n(0)}{L_p} e^{-x/L_p} \longrightarrow (4)$$

This equation verifies that the hole current decreases exponentially with distance.

The Law of the Junction:-

If the hole concentrations at the edges of the space charge region are P_p and P_n in the 'p' and 'n' materials respectively. and if the barrier potential across this depletion layer is V_B, then

$$P_p = P_n e^{V_B/V_T} \longrightarrow (5)$$

This is the Boltzmann relationship of Kinetic gas theory. It is valid even under non-equilibrium conditions as long as the net hole current is small compared with the diffusion or the drift hole current. under this condition, called "Low level Injection".

In an open circuited P-n Junction, $P_p = P_{po}$, $P_n = P_{no}$ and $V_B = V_0$. Substituting these values in eqn(5), then we obtain the contact potential V_0.

Consider now a Junction biased in the forward direction by an applied voltage 'V'. Then the barrier voltage V_B is decreased from its equilibrium value 'V_0' by the amount V, or $V_B = V_0 - V$. The hole concentration through out the p region is constant and equal to the thermal equilibrium value, or $P_p = P_{po}$. The hole concentration varies with distance into the n-side;

At the edge of the depletion layer, $x=0$, $P_n = P_n(0)$. Therefore

$$P_{p0} = P_n(0) e^{(V_0 - V)/V_T} \longrightarrow (6)$$

Since $$P_{p0} = P_{no} e^{V_0/V_T} \longrightarrow (7)$$

By combining eqn's (6) & (7), we obtain

$$P_n(0) = P_{no} e^{V/V_T} \longrightarrow (8)$$

for a forward Bias ($V>0$), the hole concentration $P_n(0)$ at the Junction is greater than the thermal equilibrium value P_{no}. Similarly we obtain for electrons.

The hole concentration $P_n(0)$ injected into the n-side at the Junction is obtained by substituting eqn (8) in eqn(2), yielding

$$\boxed{P_n(0) = P_{no}(e^{V/V_T} - 1)} \longrightarrow (9)$$

forward Currents:- The hole current $I_{pn}(0)$ crossing the junction into the n-side is given by eqn(9), with $x=0$. Using eqn(9) for $P_n(0)$, we obtain

$$I_{pn}(0) = \frac{Aq D_p P_{no}}{L_p}\left(e^{V/V_T}-1\right) \longrightarrow (10)$$

The electron current $I_{np}(0)$ crossing the junction into the p-side is obtained from eqn(10) by interchanging 'n' and 'p', or

$$I_{np}(0) = \frac{Aq D_n n_{po}}{L_n}\left(e^{V/V_T}-1\right) \longrightarrow (11)$$

Since the total diode current I is the sum of $I_{pn}(0)$ and $I_{np}(0)$, or

$$I = I_0\left(e^{V/V_T}-1\right) \longrightarrow (12)$$

where

$$I_0 = \frac{Aq D_p P_{no}}{L_p} + \frac{Aq D_n n_{po}}{L_n} \longrightarrow (13)$$

If W_p and W_n are the widths of the 'p' and 'n' materials respectively, the above derivation has implicitly assumed that $W_p \gg L_p$ and $W_n \gg L_n$.

Reverse saturation Current:-

for a reverse bias whose magnitude is large compared with V_T [$\approx 26mV$ at room temp^n], $I \to -I_0$. Hence I_0 is called the "Reverse saturation Current".

Since from Mass Action Law, $P_p n_p = n_i^2$, $P_n n_n = n_i^2$

and $P_p = N_A$, $n_n = N_D$ $\quad n_p = \frac{n_i^2}{N_A}$, $\quad P_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D}$

$\therefore$ Eqn(13) can be written as,

$$I_0 = Aq\left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right] n_i^2 \longrightarrow (14)$$

where $n_i^2 = A_0 T^3 e^{-E_{g0}/kT} = A_0 T^3 e^{-V_{g0}/V_T}$ $\longrightarrow (15)$

where

$V_{g0} \to$ Voltage which is numerically equal to the forbidden gap energy E_{g0} in electron volts

$V_T \to$ Volt equivalent of temp^n.

for Ge, the diffusion constants D_p and D_n vary approximately inversely proportional to T. Hence the temperature dependence of I_0 is

$$I_0 = K_1 T^2 e^{-V_{g0}/V_T} \longrightarrow (16)$$

where $K_1 \rightarrow$ constant Independent of temp^n.

This is valid for Ge only, in this we have neglected carrier generation and recombination. for the Si, the diffusion current is negligible compared with the transition layer charge generation current, which is given approximately by ***

$$\boxed{I = I_0 \left(e^{V/\eta V_T} - 1\right)}$$

where $\eta = 2$ for small (rated) currents and $\eta = 1$ for large currents.

Volt-Ampere characteristics of P-n Junction Diode:-

Since we know the relation between V & I is

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

→ when the applied voltage 'V' is greater than zero i.e, when we connect diode in forward Bias,

$$V = +V,$$

$$\therefore I = I_0 \left(e^{\frac{V}{\eta * 26} \times 10^3} - 1\right)$$

Since $V_T = 26mv$ at $300^\circ k$

$\therefore e^{\frac{10^3 V}{26\eta}} >> 1$, so we can write

$$I = I_0 e^{\frac{V \times 10^3}{\eta * 26}}$$

where $\eta = 1$ for Ge
$\eta = 2$ for Si

From the above eqn, current in a diode depends on the applied voltage only because I_0 & η are constants.

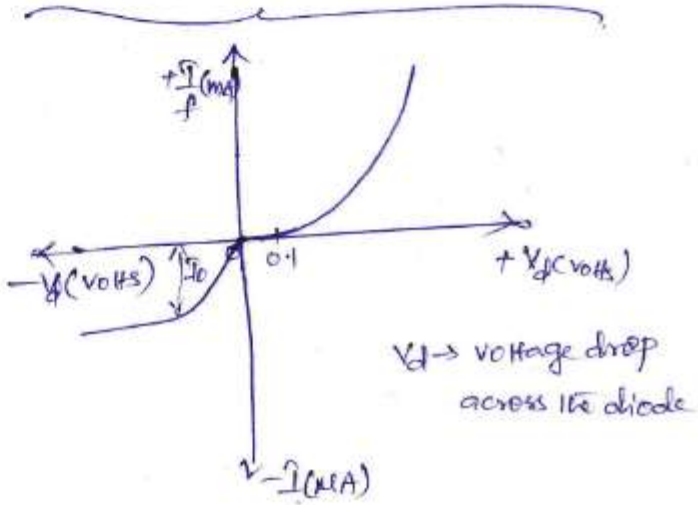
I_0 increases exponentially with the voltage.

→ when the applied voltage is less than zero i.e, when the diode connected in Reverse Bias, $V \rightarrow -V$

$$\therefore I = I_0 \left(e^{\frac{-V \times 10^3}{\eta \times 26}} - 1\right)$$

Here $e^{\frac{-V \times 10^3}{\eta \times 26}} << 1$, $\therefore \boxed{I \simeq -I_0}$

The reverse current (I_0) is constant, Independent of the applied reverse bias. Consequently, I_0 is referred to as the "Reverse Saturation Current".



Cut in voltage (V_γ):-

→ The minimum forward voltage required for the conduction to takes place is called "Cut in voltage" of the diode.

→ Cut in voltage also called 'offset voltage' as 'Threshold voltage' or 'Knee voltage' or 'Break voltage'.

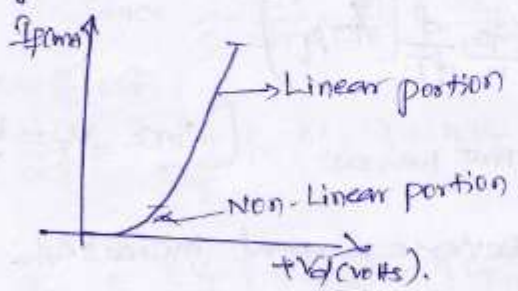
→ If the applied voltage is below Cut in voltage, forward current is zero i.e. $I_f = 0$.

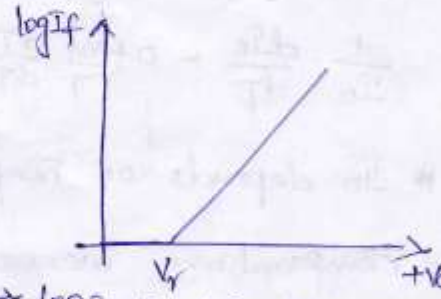
→ Cut in voltage decreases with the temperature.

→ for $1^\circ c$, V_γ decreases by 2-3mV.

→ from the Diode characteristics, Diode is a non linear device, Active component and also unidirectional device.

→ When diode is Reverse Biased, the reverse voltages always must be less than breakdown voltage of the device. Otherwise the normal diode will be destroyed.

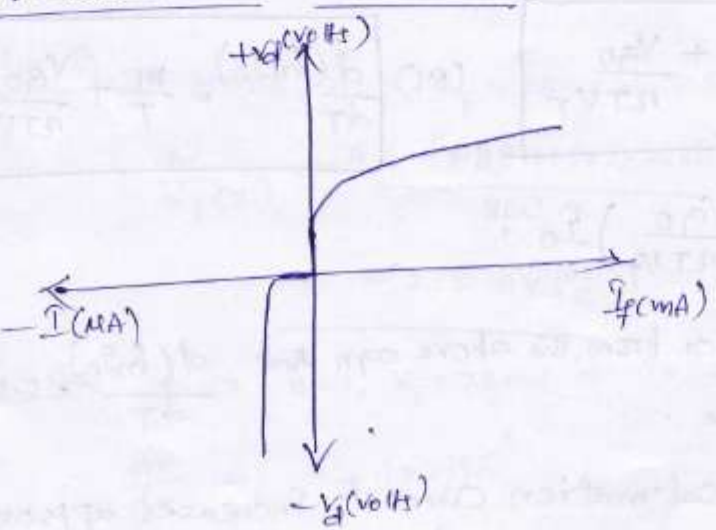




→ log If Vs Vd curve represents a straight line.

→ ohms law is applied to the diode only for the linear portion of the characteristics.

I-V characteristics of Diode:-



$I_0 = K_1 T^2 e^{-V_{G0}/\eta V_T}$ ⟶

where K_1 → constant independent of temp^n.

Temperature Dependence of p-n characteristics :—

Since we know the formula for the reverse saturation current as Minority carrier Current $-(I_0)$ is

$$I_0 = K T^m e^{-V_{G0}/\eta V_T} \longrightarrow (1)$$

where K → constant, V_{G0} → forbidden Gap in Volts

for Ge: $\eta = 1$, $m = 2$, $V_{G0} = 0.755\ V$

for Si: $\eta = 2$, $m = 1.5$, $V_{G0} = 1.21\ V$

By taking the log derivative of the logarithm of eqn(1), we have

$$\ln(I_0) = \ln(K) + m\ln(T) + \ln\left(e^{-V_{G0}/\eta V_T}\right)$$

$$\ln(I_0) = \ln(K) + m\ln(T) - \frac{V_{G0}}{\eta V_T}$$

By derivating with respect to 'T':

$$\frac{1}{I_0}\cdot\frac{dI_0}{dT} = 0 + \frac{m}{T}\frac{dT}{dT} - \frac{V_{G0}}{\eta}\frac{d}{dT}\left[\frac{1}{KT/q}\right]$$

[* I_0 depends on Temperature i.e., as the temperature increases Reverse Current increases.] [since $V_T = \frac{KT}{q}$]

$$\therefore \frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} - \frac{V_{G0}}{\eta}\times\frac{q}{K}\cdot -1/T^2 \qquad \frac{d}{dT}\left[\frac{1}{T}\right] = -\frac{1}{T^2}$$

$$\frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T}\cdot\frac{q}{KT} \Rightarrow \frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T V_T}$$

$$\boxed{\frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T V_T}} \quad (\text{or}) \quad \boxed{\frac{d(\ln I_0)}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T V_T}}$$

$$\frac{dI_0}{dT} = \left(\frac{m}{T} + \frac{V_{G0}}{\eta T V_T}\right) I_0 .$$

At room temp^n, we deduce from the above eqn that $\frac{d(\ln I_0)}{dT} = 0.08^{\circ}C^{-1}$ for Si and $0.11^{\circ}C^{-1}$ for Ge.

→ we find that the reverse saturation current increases approximately 7% per °C for both Si & Ge. Since $(1.07)^{10} \approx 2.0$. We conclude that the reverse saturation current approximately doubles for every 10°C rise in temp.

from the diode current- eqn,

$$I = I_0 (e^{V/\eta V_T} - 1) \longrightarrow (1)$$

By applying logarithm on both the sides

$$\Rightarrow \ln(I/I_0) = V/\eta V_T$$

$$\Rightarrow V = \eta V_T * \ln(I/I_0) = \eta \frac{KT}{q} \cdot \ln(I/I_0) \longrightarrow (2)$$

By differentiating above eqn w.r.t to T, we get the variation in voltage with respect to T.

$$\frac{dV}{dT} = \frac{\eta K}{q} \frac{d}{dT}\left[T \cdot \ln(I/I_0)\right] \quad \left[\because T \& I_0 \text{ are variable w.r.t. } T\right]$$

$$\frac{dV}{dT} = \frac{\eta K}{q}\left[\ln(I/I_0) + T \cdot \frac{1}{I/I_0} \cdot \frac{-I}{I_0^2}\frac{dI_0}{dT}\right]$$

$$= \frac{\eta K}{q}\left[\ln(I/I_0) - \frac{T}{I_0}\frac{dI_0}{dT}\right] = \frac{\eta K * T}{\eta q}\ln(I/I_0) - \frac{\eta K T}{q I_0}\frac{dI_0}{dT}$$

$$\frac{dV}{dT} = \frac{\eta V_T}{T}\ln(I/I_0) - \frac{\eta K T}{q}\left[\frac{1}{I_0}\frac{dI_0}{dT}\right] \longrightarrow (3)$$

Since $\frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T V_T} \longrightarrow (4)$

from (3) & (4),

$$\therefore \frac{dV}{dT} = \frac{\eta V_T}{T}\ln(I/I_0) - \eta V_T\left[\frac{m}{T} + \frac{V_{G0}}{\eta T V_T}\right]$$

$$\frac{dV}{dT} = \frac{\eta V_T}{T}\ln(I/I_0) - \eta V_T \frac{m}{T} - \frac{V_{G0}}{T} \longrightarrow (5)$$

from eqn (2) & (5)

$$\frac{dV}{dT} = \frac{V}{T} - \frac{V_{G0}}{T} - \frac{m\eta V_T}{T} = \frac{V - \left[V_{G0} + m\eta V_T\right]}{T}$$

for Si:- $m = 1.5$, $\eta = 2$, $V_T = 26\,mV$ at $T = 300K$, $V = 0.6V$ [cut in voltage]

$V_{G0}(Si) = 1.21$ volts

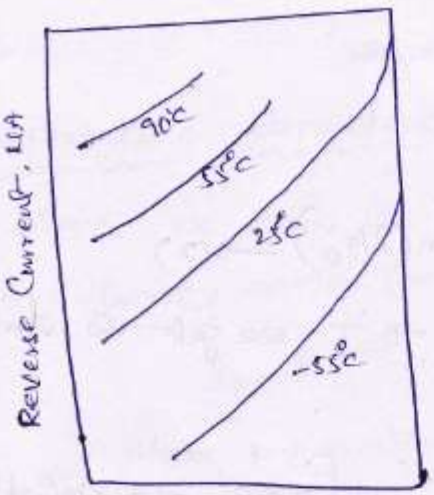
$$\therefore \frac{dV}{dT}(Si) = \frac{0.6 - [1.21 + 1.5 * 2 \times 26 \times 10^{-3}]}{300}$$

$$= -2.2\,mV/^\circ C$$

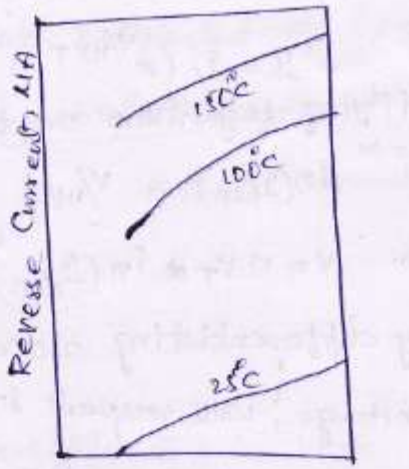
for Ge:- $m = 2$, $\eta = 1$, $V_T = 26mV$ at $T = 300K$, $V = 0.2V$, $V_{G0} = 0.785$ volts.

$$\frac{dV}{dT} = -2.1\,mV/^\circ C$$

i. on average, $\frac{dV}{dT} = -2.5\,mV/^\circ C$.



(a) Germanium Diode



(b) Silicon Diode

Ideal Versus practical (characteristics) Resistance Levels :-

Static Resistance :-

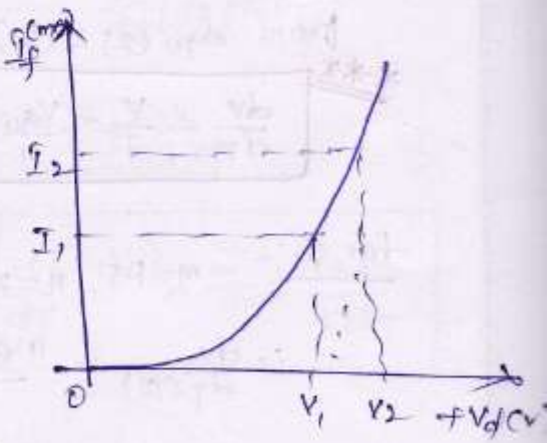
The static Resistance R of a diode is defined as the ratio V/I of the voltage to the current.

→ At any point on the volt-Ampere characteristics of the diode, the resistance R is equal to the reciprocal of the slope of a line joining the operating point to the origin.

→ The static resistance varies widely with V and I and is not a useful parameter. $\underline{\text{at } V_1}$ $R = \frac{V_1}{I_1}\ \Omega$ $\underline{\text{at } V_2}$ $R = \frac{V_2}{I_2}\ \Omega$

Dynamic resistance :-

→ It is defined as the reciprocal of the slope of the volt-Ampere characteristic, $r = \frac{dV}{dI}$.



→ The Dynamic resistance is not a constant, but depends upon the operating voltage.

→ Dynamic resistance $r_d = \frac{dV}{dI} = \frac{V_2 - V_1}{I_2 - I_1} = \frac{1}{\text{slope of V-I characn.}}$

→ We know the Current expression is

$$I = I_0\left(e^{V/\eta V_T} - 1\right) \Rightarrow \ln(I/I_0) = \frac{V}{\eta V_T} \Rightarrow \boxed{V = \eta V_T \ln(I/I_0)}$$

By differentiating the above eqn with respect to 'I' then

$$\frac{dv}{dI} = \eta V_T \frac{d[\ln[I/I_0]]}{dI} = \eta V_T * \frac{1}{I/I_0} * \frac{1}{I_0} = \frac{\eta V_T}{I}$$

$$\boxed{\frac{dv}{dI} = \frac{\eta V_T}{I}} = r_d$$

$$\therefore \boxed{r_d = \frac{\eta V_T}{I}}$$

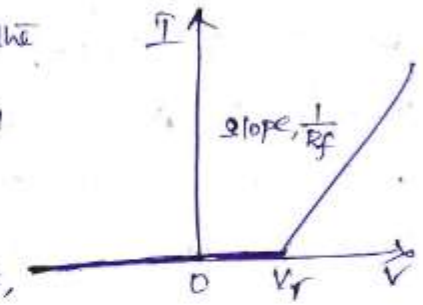
* → Dynamic resistance varies inversely with current.

→ At room temp, $\eta = 1$, $r = 26/I$ for Ge.

where I is in mA, r_d is in ohms.

Piecewise Linear Diode characteristics:

for a large signal approximation, piecewise linear results.



→ from the figure, the Break point is not at the origin and hence V_γ is also called the "offset", or "threshold" voltage.

→ The diode behaves like an open circuit if $V < V_\gamma$, and has a constant incremental resistance $r = dV/dI$ if $V > V_\gamma$.

Transition and Diffusion Capacitances:

(i) Transition Capacitance (C_T): also called space charge capacitance.

When a reverse bias is applied to a p-n junction diode, negative charge is developed on the p-side and similarly positive charge on the n-side.

Before reverse Bias is applied, because of concentration Gradient there is some space charge region. The thickness of the barrier increases with reverse Bias. So space charge increases as reverse bias voltage increases.

But $C = \frac{Q}{V}$, therefore $C_T = \left|\frac{dQ}{dV}\right|$

where dQ → Magnitude of charge increase due to voltage 'dv'.

Since we know that $I = \frac{dQ}{dt}$

Therefore, if the voltage 'dv' is changing in time dt, then a current will result

given by $\boxed{I = C_T \frac{dV}{dt}}$ $\left[\because I = \frac{dQ}{dt} = \frac{dQ}{dV} * \frac{dV}{dt} \quad I = C_T \frac{dV}{dt}\right]$

if 'V' is constant (i.e. DC), $I = 0$.

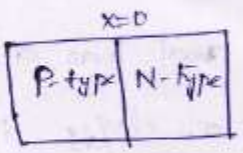
So this current is exists for AC only.

$C_T \rightarrow$ Transition region capacitance or space charge capacitance or barrier capacitance or depletion region capacitance.

$\rightarrow$ This capacitance is not constant but depends on Reverse Bias.

Alloy Junction :—

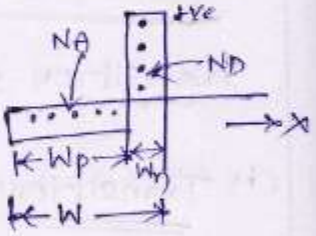
Let us take a trivalent impurity ex: Indium. If this is placed against n-type Ge, and heated to a high temperature, Indium diffuses into the Ge crystal, a p-n junction will be formed and for such a junction there will be abrupt change from acceptor ions on one side to donor ions on the other side. Such a junction is called 'Alloy Junction" or "Diffusion Junction". There is sudden change in concentration levels.



To satisfy the condition of charge neutrality,

$$\boxed{q N_A W_p = q N_D W_n}$$

[i.e, charge on either side of the junction is equal].



$\rightarrow$ If $N_A << N_D$, then $W_p >> W_n$. The width of the region W_n very small. So it can be neglected. So we can assume that the entire barrier potential appears across the p-region just near the junction.

From poisson's equation,

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\epsilon} \Rightarrow \frac{dV}{dx} = \frac{qN_A}{\epsilon} x, \Rightarrow \boxed{V = \frac{qN_A}{\epsilon} * \frac{x^2}{2}}$$

At $x = W_p$, $V = V_B$, $W_p = W$

$$\therefore \boxed{V_B = \frac{qN_A}{2\epsilon} * W^2}$$

From the above eqn, the value of 'W' depends upon the applied reverse bias 'V' and Barrier voltage V_B depends on the width 'W'. indirectly, V_B changes as V changes. i.e, $V_B = V_0 - V$,

V $\rightarrow$ reverse Bias voltage with negative sign.

As voltage increases, width increases and V_B increases.

$$W \propto \sqrt{V_B}$$

If 'A' is the Area of the junction, the change in the width 'W' is

$$Q = q N_A W A$$

Where WxA = volume, $q \times N_A$ = Total charge density

$$C_T = \frac{dQ}{dV} = q N_A \cdot A \cdot \left|\frac{dW}{dV}\right| \qquad \because W = \sqrt{\frac{2\epsilon V}{q N_A}}$$

$$Q = q N_A \sqrt{\frac{2\epsilon V}{q N_A}} \cdot A = \sqrt{q N_A} \times \sqrt{2\epsilon V_B} \cdot A \qquad W \propto \frac{1}{N_A}$$

$$W = \sqrt{\frac{2\epsilon V_B}{q N_A}}, \quad \frac{dW}{dV} = \frac{1}{2}\sqrt{\frac{2\epsilon}{q N_A}} (V_B)^{-1/2}$$

But $\sqrt{V_B} = W\sqrt{\frac{q N_A}{2\epsilon}}$

$$\frac{dW}{dV} = \frac{1}{2}\sqrt{\frac{2\epsilon}{q N_A}} \times \frac{\sqrt{2\epsilon}}{\sqrt{q N_A W}} = \frac{\epsilon}{q N_A} \times \frac{1}{W} = \frac{\epsilon}{q N_A W}$$

Since $C_T = q N_A * A * \frac{dW}{dx} = q N_A \cdot A \cdot \frac{\epsilon}{q N_A W}$

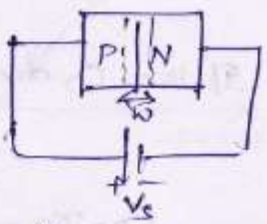
$$\boxed{C_T = \frac{\epsilon A}{W}}$$

This expression is similar to that of the parallel plate capacitor.

(ii) Diffusion Capacitance:—

When a p-n junction diode is in forward Bias, the junction capacitance will be much larger than the transition capacitance (C_T).

When the diode is in forward Biased, Barrier potential is reduced. Holes from p-side are injected into the n-side from p-region. This injected charge is proportional to the applied forward Bias voltage 'v'. So the rate of change of injected charge 'Q' with voltage 'V' is called the 'Diffusion capacitance' (C_D).



Derivation for C_D:—

Assume that p-side is heavily doped compared to n-side.

∴ holes injected from 'p' to 'n' > Electrons injected from 'n' to 'p'

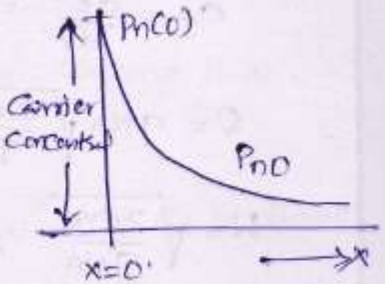
As $V_s \uparrow \rightarrow W \downarrow \rightarrow V_B \downarrow$

as $W \downarrow \rightarrow C \uparrow$

so we can say that the total diode current is mainly due to holes only. so the excess charge due to minority carriers will exist only on n-side.

The total charge Q is equal to the Area under the curve multiplied by the charge of electrons and the cross sectional Area (A) of the diode.

$P_n(0)$ is the concentration of holes/cm^3. Area in cm^2, x in cm.



$$Q = \int_0^\infty Aq\, P_n(0)\, e^{-x/L_p}\, dx = Aq\, P_n(0) \int_0^\infty e^{-x/L_p}\, dx$$

$$Q = Aq\, P_n(0) \cdot \frac{e^{-x/L_p}}{-1/L_p}\Bigg|_0^\infty = -Aq\, L_p\, P_n(0)\,[0-1]$$

$$Q = Aq\, L_p\, P_n(0)$$

$$C_D = \frac{dQ}{dV} = Aq\, L_p \frac{dP_n(0)}{dV} \longrightarrow (1)$$

We know that, $I_{pn}(x) = \frac{qA\, D_p\, P_n(0)\, e^{-x/L_p}}{L_p}$ (or) $I_{pn}(0) = I = \frac{Aq\, D_p\, P_n(0)}{L_p}$

$$P_n(0) = \frac{L_p * I}{Aq D_p}$$

$$\frac{dP_n(0)}{dV} = \frac{L_p}{Aq D_p} \cdot \frac{dI}{dV} = \frac{L_p}{Aq D_p} \cdot g \longrightarrow (2)$$

g → conductance of the diode

from ① & ②.

$$C_D = Aq\, L_p \cdot \frac{L_p}{Aq D_p} \cdot g = \frac{L_p^2}{D_p} \cdot g$$

The Life time of holes, $\tau_p = \tau$ is given by the equation

$$\boxed{\tau = \frac{L_p^2}{D_p}}$$

where D_p → Diffusion Constant of holes

L_p → Diffusion Length of holes

D_p → cm^2/sec

$$\therefore \boxed{C_D = \tau \times g}$$

But Diode Resistance, $r = \frac{\eta V_T}{I}$

$$\therefore g = \frac{I}{\eta V_T}$$

$$\therefore \boxed{C_D = \frac{I\tau}{\eta V_T}}$$ due to holes only.

If the C_D due to electrons represented as C_{Dn}.

$$\therefore \boxed{C_D = C_{Dp} + C_{Dn}}$$

$$C_D = \tau g \Rightarrow C_D = \frac{\tau}{r} \Rightarrow \boxed{r * C_D = \tau}$$

→ $r * C_D$ is called "Time Constant of the diode".

$\therefore Q = A q L_p P_n(0)$ & $I = \frac{A q D_p P_n(0)}{L_p}$

$\Rightarrow \frac{Q}{L_p} = A q P_n(0)$ $\therefore I = \frac{D_p * Q}{L_p^2}$

But $\frac{L_p^2}{D_p} = \tau$ $\therefore \boxed{I = \frac{Q}{\tau}}$

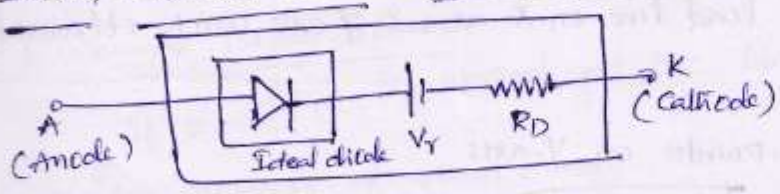
Diffusion capacitance, $C_D = \frac{I\tau}{nV_T}$.

Ideal Versus practical characteristics:-

parameter	units	Ideal diode	practical diode
forward Resistance (R_f)	Ω	0	10Ω to 100Ω's
Reverse Resistance (R_r)	Ω	∞	kΩ to MΩ
Cut in voltage (V_γ)	volts	0	Si: 0.6V, Ge: 0.2V
Reverse Current (I_r)	μA	0	100μA.

Diode Equivalent Circuits:-

Ideal characteristics of a p-n junction:-



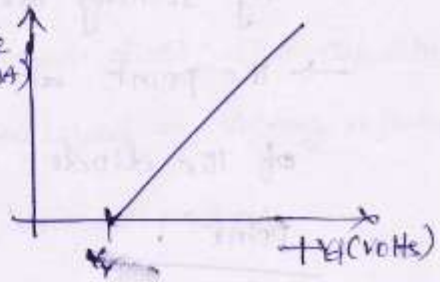
for an ideal diode, the cut in voltage (V_γ) = 0.

→ The p-n junction diode will conduct after the cut in voltage V_γ. It is the minimum voltage beyond which diode starts conduction.

Piecewise Linear characteristics of a p-n diode:-

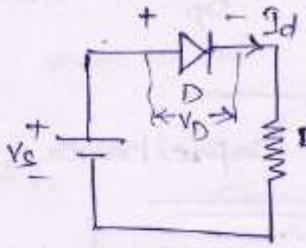
The diode current eqn is $I = I_0(e^{V/\eta V_T} - 1)$.

Diode Current I varies with the voltage across it exponentially. But for small variations, it is approximated to be linear. Such a characteristics is called "Piecewise Linear characteristics of a diode".



Load Line Analysis:—

The piecewise linear characteristics of the diode will not provide accurate results. So the actual variation of V-I characteristics of is to be considered.



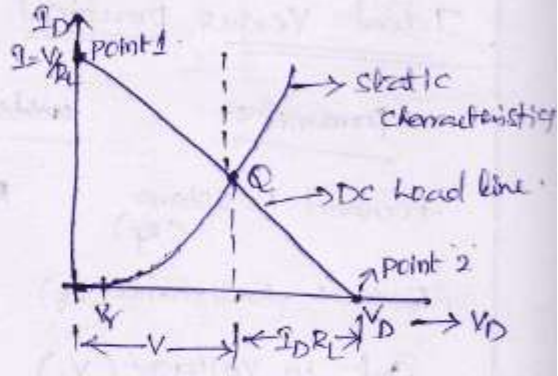
from the diagram

$$V_s = V_d + I_D R_L \Rightarrow I_D = \frac{V_s - V_D}{R_L}$$

Since V_D & R_L are fixed. when diode starts conducting then $\frac{-V_D}{R_L} = C$ [constant]

Hence $I_D = \frac{V_s}{R_L} + C$

This can be compared with standard equation of straight line, $y = mx + c$.



→ for a given supply voltage V_s, the lower value of the load resistance R_L will have steeper load line and results in the higher value of quiscent current.

Using the equation, $V_s = V_D + I_D R_L$

The two points of the load line on X-axis & Y-axis can be obtained.

Point 1 is:

when $V_D = 0$ i.e, point on Y-axis

$$\therefore V_s = I_D R_L \Rightarrow \boxed{I_D = \frac{V_s}{R_L}}$$

Point 2: when $I_D = 0$ i.e, point on x-axis is

$$V_s = V_D \Rightarrow \boxed{V_D = V_s}$$

By joining these two points 1 & 2 we get the DC load line.

→ The point at which the load line intersects the V-I characteristics of the diode is called the "Quiescent point" (or) "operating point".

Breakdown Mechanisms in Semiconductor Diodes:—

There are three types of mechanisms in semiconductor devices

(i) **Avalanche Breakdown:**

When the number of carriers are large, the current flowing through the diode which is proportional to free carriers, also increases. when this current is large "Avalanche Breakdown" will occur.

→ When there is no bias applied to the diode, there are certain number of thermally generated carriers.

(ii) **Zener Breakdown:**

If the Electric field is very strong to disrupt or break the covalent bonds, there will be sudden increase in the number of free carriers and hence large current and consequent breakdown.

If thermally generated carriers do not have sufficient energy to break the covalent bonds. If the Electric field is very high then covalent bonds are directly broken. This is "Zener Breakdown".

→ If the doping concentration is high, the depletion region is narrow and will have high field intensity to cause Zener Breakdown.

(iii) **Thermal Breakdown:**

If the diode is biased and the bias voltage is well with in the breakdown voltage at room temp, there will be certain amount of current which is less than the breakdown current. Now keeping the bias voltage as it is, if the temperature increases due to thermal energy more no of carriers will be produced and finally breakdown will occur. This is called "Thermal Breakdown".

** Diodes which are designed with adequate power dissipation capabilities to operate in the break down region may be employed as voltage reference or constant voltage devices. Such devices are knownas "Avalanche & Zener diodes".

Zener Diode characteristics:-

→ When the reverse voltage reaches breakdown voltage in normal PN junction diode, the current through the junction and the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. one such diode is known as 'zener diode'.

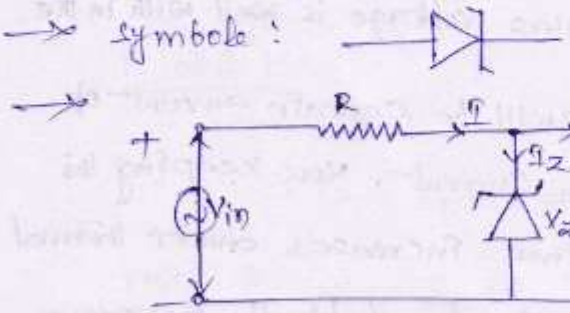
→ zener diode is heavily doped than the ordinary diode.

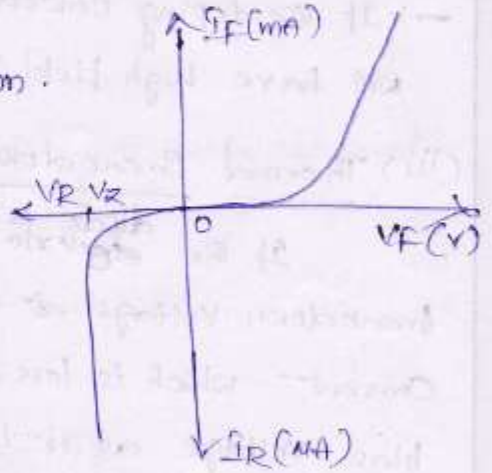
→ The operation of zener diode is same as that of ordinary PN diode under the forward-biased condition. Whereas under reverse biased condition, breakdown of the junction occurs. The breakdown voltage depends upon the amount of doping. If the diode is heavily doped depletion region will be thin and breakdown occurs at lower reverse voltage and further the breakdown voltage is sharp. whereas a lightly doped diode has a higher breakdown voltage. Thus breakdown voltage can be selected with the amount of doping.

→ The sharp increasing current under breakdown conditions are due to the following two mechanisms.

(1) Avalanche Breakdown (2) Zener Breakdown.

→ Symbol:





→ Applications:-

→ When it is required to provide constant voltage across load resistance R_L, the input voltage may be varying over a range. As shown, zener diode is reverse biased and as long as the input voltage does not fall below V_Z (zener breakdown voltage), the voltage across the diode will be constant and hence the load voltage will also be constant. So it is used in voltage Regulators.

Tunnel Diode:—

A P-n junction diode of the type has an impurity concentration of about 1 part in 10^8. With this amount of doping the width of the depletion layer which constitutes a potential barrier at the junction is of the order of 5 microns i.e. 5×10^{-4} cms. This potential barrier restrains the flow of carriers from the side of the function where they constitutes majority carriers to the side where they constitute minority carriers.

→ If the concentration of impurity atom is greatly increased to 1 part 10^3, the device characteristics are completely changed.

→ This new diode was announced in 1958 by Esaki. So this Tunnel diode also called "Esaki diode".

Tunneling phenomenon:—

→ The width 'W' of the barrier is inversely related to the square root of the impurity concentration i.e.

$$W \propto \frac{1}{\sqrt{\text{Impurity concentration}}}$$

Therefore the width of the Barrier reduced to less than 100A [i.e, 10^{-6} cm] from 5 microns. This thickness is one fiftieth the wavelength of visible light.

→ A particle must have an energy atleast equal to the height of potential energy Barrier if it is to move from one side of the Barrier to the other.

→ from schrodinger equation, for this Esaki diode, indicates that there is a large probability that an electron will penetrate through the Barrier. This quantum ~~probability~~ mechanism is referred to as "Tunneling" and hence these impurity density P-n junction devices are called "Tunnel diodes".

Principle and operation :—

→ Tunnel diode is working on the principle of "Tunneling phenomenon".

→ Energy Band structure of a Highly doped p-n diode:

It is required that occupied energy states exist on the one side from which the electron tunnels and that allowed energy states [i.e. Empty states] exist on the other side at the same energy level. Here we must consider the energy band structure when the impurity Concentration is very high.

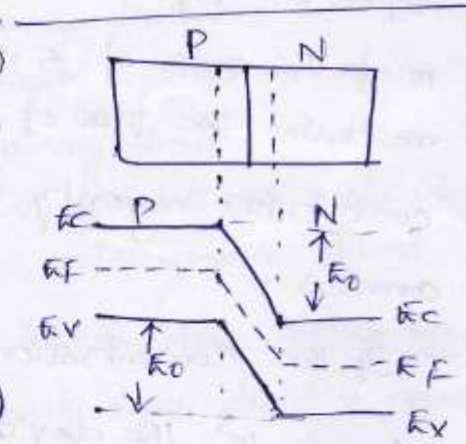


figure shows the energy Band diagram for Moderately doped.

→ for a lightly or moderately doped p-n diode fermi Level "Ef" lies inside the forbidden energy Gap.

→ for a diode which is doped heavily enough to make tunneling possible, (Ef) fermi level lies out-side the forbidden Band Gap.

$$E_f = E_c - KT \ln\left(\frac{N_c}{N_D}\right) \quad , \quad E_f = E_v + KT \ln\left(\frac{N_v}{N_A}\right)$$

→ If for a lightly doped semiconductor, $N_D < N_c$ so that $\ln\left(\frac{N_c}{N_D}\right)$ is positive number. Hence $E_f < E_c$ and the fermi Level lies inside the forbidden Band gap.

→ If donor concentration increases i.e, If $N_D > N_c$, then $\ln\left(\frac{N_c}{N_D}\right)$ is negative. Hence $E_f > E_c$ and the fermi Level in the n-type material lies in the conduction Band.

similarly, if Acceptor concentration increases i.e $N_A > N_v$, so that $\ln\left(\frac{N_v}{N_A}\right)$ is negative. Hence $E_v > E_f$ and the fermi Level in the p-type material lies in the Valence Band.

→ Since we have formulae for E_g and E_o i.e,

$$E_g = KT \ln\left(\frac{N_c N_v}{n_i^2}\right) \qquad E_o = KT \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

Here $N_D > N_c$ & $N_A > N_v$ so $E_o > E_g$.

The contact difference of potential Energy E_0 exceeds the forbidden Energy Gap Voltage (E_g).

case(i) Open Circuit condition :—

In an open circuit condition, the band structure of a heavily doped p-n junction must be as the fermi Level (E_f) in the p-side is at the same energy level as the fermi Level in the n-side.

→ We observe that, there are no filled states on one side of the junction which are at the same energy as empty allowed states on the other side. Hence there can be no flow of charge in either direction across the junction, and the current is zero.

→ In an open circuited condition i.e. if we do not applying either of the biasing, conduction is zero.

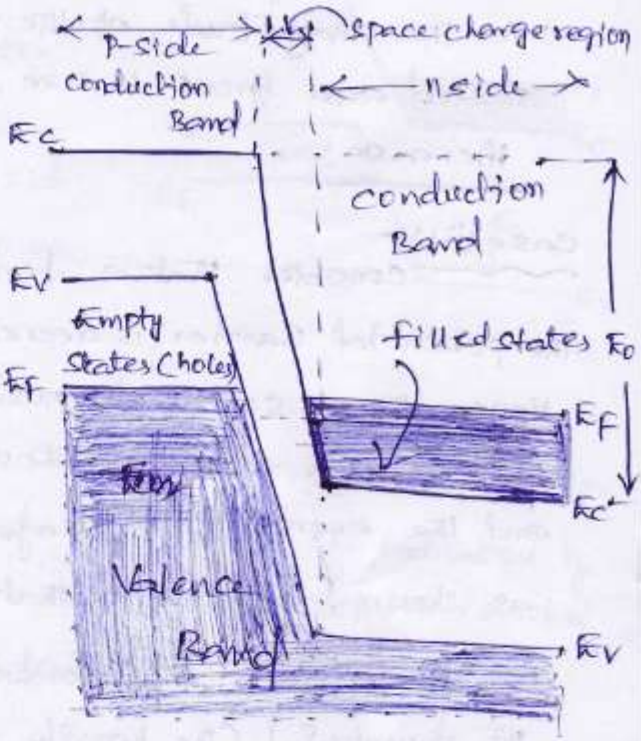


fig: open-circuited condition

case(ii) :- Reverse Bias condition :—

Let us consider that the p side material is grounded and that a voltage across the diode shifts the n-side with respect to the p-side. i.e, if a Reverse Bias voltage is applied, the height of the barrier is increased above the open circuit value E_0.

Hence the n-side level must shift downward with respect to the p-side levels. Then we observe that there are some energy states (the heavily shaded region) in the valence band of the p-side which lie at the same levels as allowed empty states in the conduction Band of the n-side. Hence these electrons will tunnel from the p-to

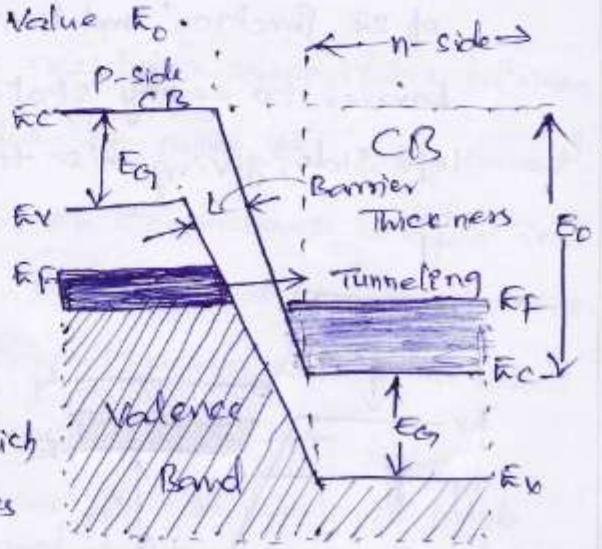


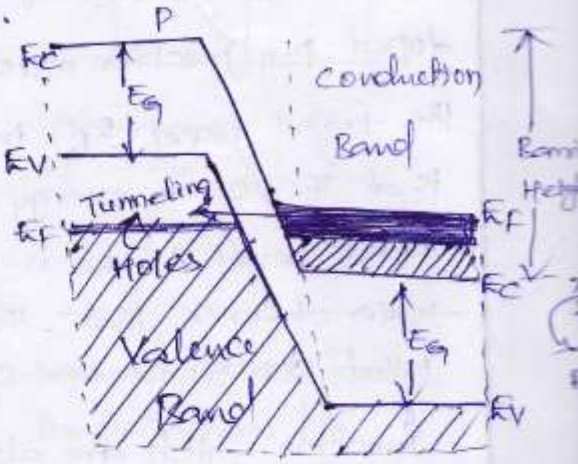
fig: Reverse Biased condition.

the n-side, giving rise to a reverse diode current.

→ As the magnitude of the reverse Bias increases, the heavily shaded area grows in size, causing the reverse current to increase.

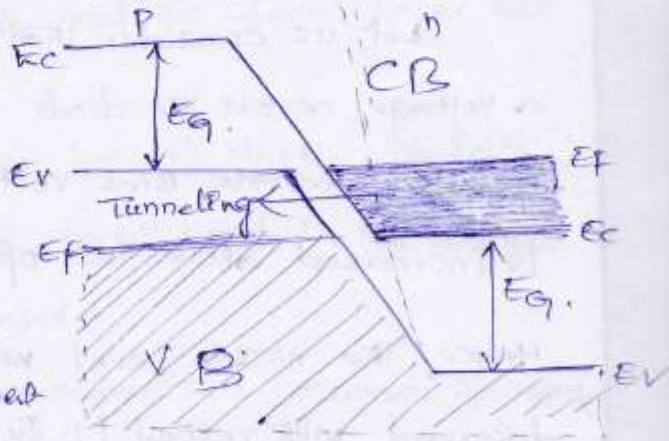
Case (iii):-

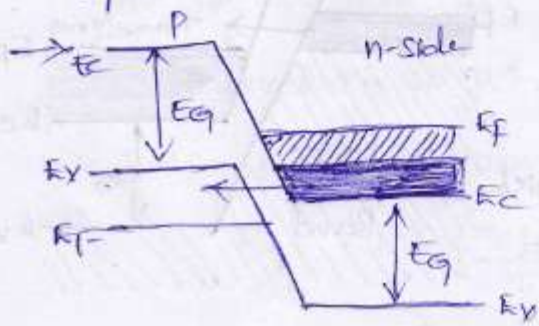
Consider that a forward Bias is applied to the diode so that the potential Barrier is decreased below E_0. Hence the n-side levels must shift upward with respect to those on the p-side, and the energy Band diagram for this as shown. We observe that there are occupied states in the conduction Band of the n-material (the heavily shaded levels). which are at the same energy as allowed empty states (holes) in the Valence Band of the p-side. Hence electrons will tunnel from the n-side to the p-side material, giving rise to the forward Current.



Forward Bias

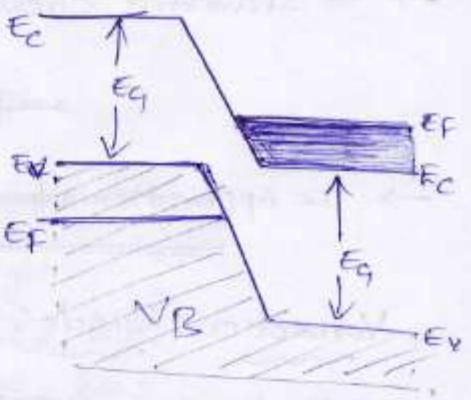
→ As the forward Bias is increased further, n-side levels shift upward. At a particular forward Biasing voltage, the occupied energy levels of occupied states in the Conduction Band of the n-material which are at the same energy as empty states in the Valence Band of p-side. Now the maximum number of electrons can leave occupied states on the right side of the function and tunnel through the barrier to empty states on the left side, giving rise to the peak Current I_p.





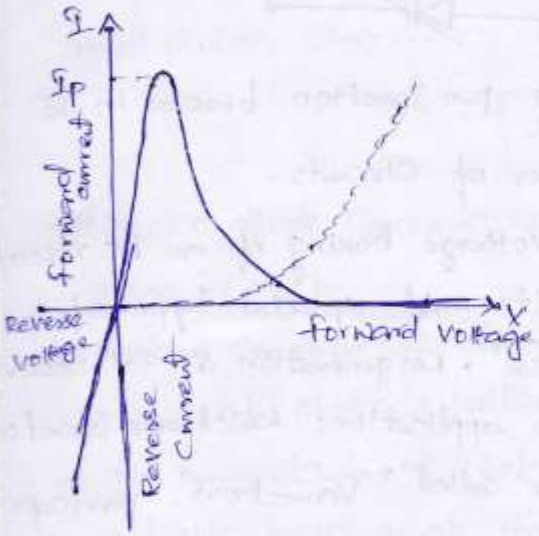
If still more forward bias is applied, position of the occupied states are at the same level of empty states. So the tunneling current decreases

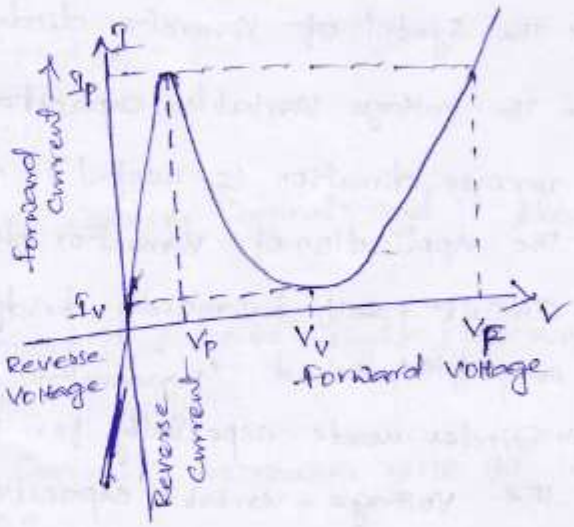
finally, at an even larger forward Bias, there are no empty allowed states on one side of the junction at the same energy as occupied states on the other side. The tunneling current must drop to zero.



Characteristics of a Tunnel Diode:—

In addition to the quantum-mechanical current, the regular P-n junction injection current is also being collected. This current is indicated by the dashed line. The resultant curve is the sum of solid and dashed curves and this resultant is the tunnel diode characteristics.





→ At the peak current I_p corresponding to the voltage V_p, the slope dI/dV of the characteristic zero. If V is increased beyond V_p, then the current decreases. As a consequence, the dynamic conductance $g = dI/dV$ is negative.

→ The tunnel diode exhibits a negative resistance characteristic between the peak current "I_p" and the minimum value "I_v", called the "valley current".

→ At the valley voltage V_v at which $I = I_v$, the conductance is again zero and beyond this point the resistance becomes and remains positive.

→ At the peak forward voltage "V_F" the current again reaches the value I_p. for larger voltages the current increases beyond this value.

→ currents whose values are between I_v and I_p, the curve is triple valued because each current can be obtained at three different applied voltages. Because of Multivalued feature it is used in "pulse and Digital circuitry".

→ The standard circuit-symbol for a tunnel diode is

→ The Application of Tunnel diode is, it is used as very high speed switch-

Varactor Diode:—

→ The barrier capacitance is not a constant but varies with applied voltage. The larger the reverse voltage, the larger is the space charge width 'W', and hence the smaller the capacitance C_T. Similarly, for an increase in forward bias (V positive), W decreases and C_T increases.

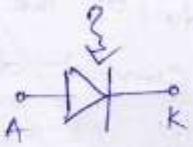
→ The symbol of Varactor diode is 

→ The voltage variable capacitance of a p-n junction biased in the reverse direction is useful in a number of circuits.

→ The Application of Varactor diode is voltage tuning of an LC resonant circuit, self balancing bridge circuits and special types of amplifiers, called 'parametric Amplifiers', FM generation & TV Receivers.

→ Diodes made especially for the above applications which are based on the voltage-variable capacitance are called "Varactors", 'Varicaps' or 'Voltacaps".

Semi-conductor photo Diode:—

→ Symbol for the Semi conductor photo diode is 

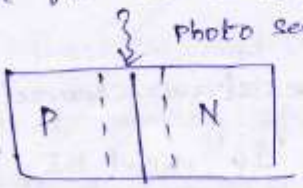
→ 

photo diode is a photo sensitive device, has high sensitivity because of photo sensitive coating is provided only at the junction.

→ principle of operation is a photo conductive effect.

→ In a photo diode, various photo sensitive materials are CdS, Se, ZnS.

→ It has a very larger depletion region. This is obtain by reducing the doping levels P&N regions.

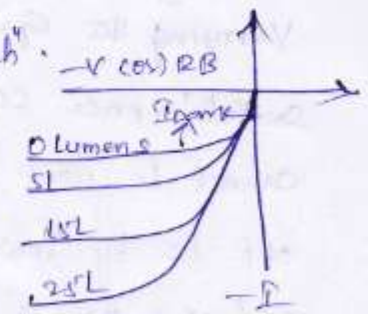
When compared to normal diode, photo diode is

→ 10 times faster
→ 100 times higher sensitivity. } advantages
→ Low power handling capability. → Disadvantage

→ Ge photo diode will respond to visible light.
→ Si photo diode will respond to Infrared light.
→ photo diode always operated under Reverse Bias.
→ The dark current of photo diode is due to minority carriers generated by the thermal energy. So Dark Current is the thermally generated current.
→ I_{photon} is the current in the photo diode due to the light energy.
→ photo diode current is the sum of thermally generated current and photon current. $I = I_D + I_{photon}$

$$I \cong I_{photon}$$

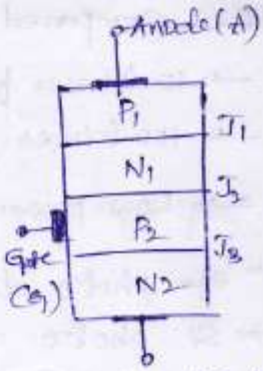
→ photo diode current is minority carrier current and it flows from 'N' to 'P'.
→ photon current is directly proportional to the light flux and number of photons falling at the junction.
→ the magnitude of photo diode current increases with the intensity of light falling at the junction.
→ photo diode current is the diffusion current.
→ photo diode basically a "light operated switch".
→ For good photo diode, the essential requirement is larger the I_{photon} to I_{dark} ratio.



Applications:—

→ As a remote control sensor.
→ In designing of opto couplers.
→ To read the Audio track recorded on motion picture film.
→ If photo diode is operating in fw Bias and light is focussed at the junction.

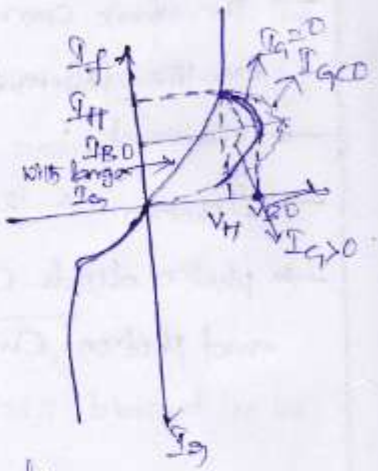
Silicon Controlled Rectifier (SCR):-



→ It is a four layer, three terminal device. In which the end p-layer acts as "Anode" and and N-layer acts as "Cathode" and p-layer nearer to Cathode acts as "Gate".

→ SCR's are made up of Si material because of leakage current in Si is less.

Characteristics of SCR's



SCR acts as switch when it is in forward Bias. When the Gate is kept open i.e, Gate Current $I_G=0$, the operation of SCR is similar to the PNPN diode. When $I_G<0$, the amount of reverse bias applied to J_2 is increased so the breakover voltage "V_{BO}" is increased.

When $I_G>0$, the amount of reverse bias applied to J_2 is decreased there by decreasing the breakover voltage. With very large positive Gate current breakover may occur at a very low voltage such that the characteristics of SCR is similar to that of ordinary PN diode.

→ The voltage at which SCR is switched ON can be controlled by varrying the Gate Current "I_G". It is commonly called as "controlled switch". once SCR is turned ON, the Gate looses control i.e, gate cannot be used to switch the device off. one way to turn the device OFF is by lowering Anode Current below the holding Current I_H by reducing the supply voltage below holding voltage V_H, keeping the Gate open.

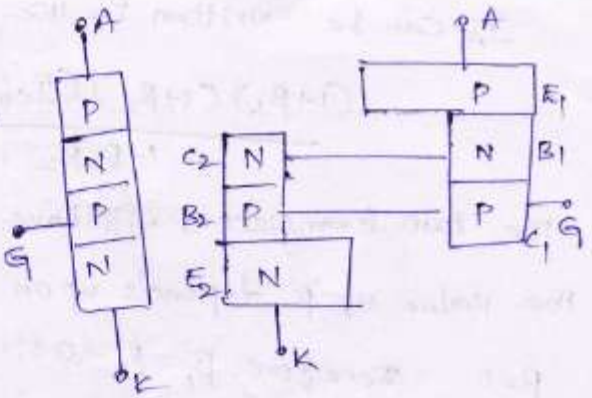
→ The Applications of SCR is, is used in relay control, phase control, heater control, battery chargers, Inverters, regulated power supplies and as static switches.

(16)

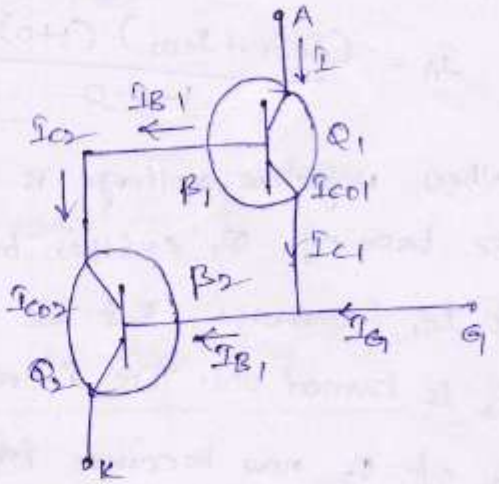
Analysis of the operation of SCR:—

It can be regarded as two transistor connected together.

The SCR can be regarded as two transistor P-N-P and N-P-N.



Suppose a +ve voltage is applied to the anode (p type) since there is no base junction injection for both the transistors, the transistors are off. The only current is the leakage current I_{co1} & I_{co2} of the two transistors. Therefore when SCR is not turned ON, the output current results is the leakage current $(I_{co1} + I_{co2})$.



In a Transistor:—

$$I_c = \beta I_B + (1+\beta) I_{co}$$

$$= \beta I_B + \beta I_{co} + I_{co} = \beta(I_B + I_{co}) + I_{co}$$

consider Transistor Q_1:

The base current of the transistor Q_1 is I_{B_1}, which is the collector current I_{c_2} of Q_2.

$$I_c = \beta(I_B + I_{co}) + I_{co}$$

$$I_{B1} = I_{c2}$$

$$\therefore I_{c_1} = \beta_1 (I_{c2} + I_{co1}) + I_{co1}$$

consider Transistor Q_2:

The base current of transistor Q_2 is the collector current I_{c_1} of Q_1.

$$I_{c_2} = \beta_2 (I_{c_1} + I_{co2}) + I_{co2}$$

Anode current is, $I_\Theta = I_{B2} + I_{c_2}$

But $I_{B2} = I_{c1}$.

$$\therefore I_A = I_{c_1} + I_{c_2}$$

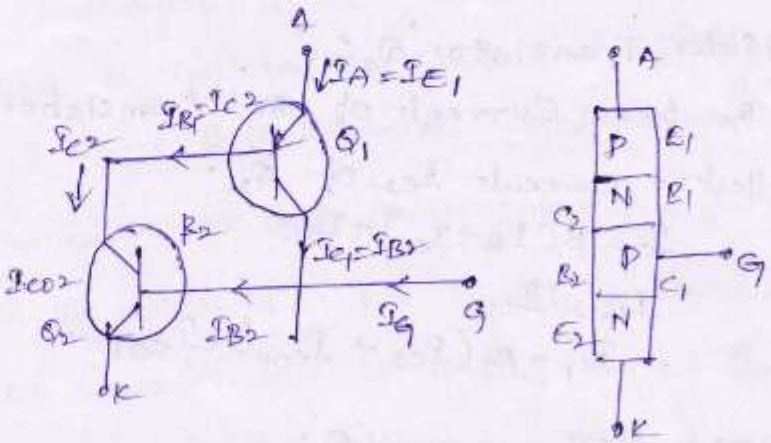
I_A can be written in the form is,

$$\frac{(1+\beta_1)(1+\beta_2)(I_{co1}+I_{co2})}{1-\beta_1\beta_2}$$

The two transistors will have wide base regions. so β will be small. The value of β depends upon the value of I_E. When I_E is very small $\beta=0$. therefore $\beta_1=\beta_2=0$.

$$I_A = \frac{(I_{co1}+I_{co2})(1+0)(1+0)}{1-0\cdot0} \approx \underline{I_{co1}+I_{co2}}$$

When Negative voltage is applied from gate to cathode to inject holes into the base of Q_1, emitter base junction of Q_1 is forward Biased. so I_{c_1} increases. But this is the base Current for Q_2. So transistor Q_2 is turned ON. This increases Collector and Emitter Currents. the I_{c_2} of Q_2 now becomes trigger current and so increase I_{c_1}. so the action is one of internal regeneration feed back, until both the transistors are driven into saturation. once the SCR is turned ON, removal of Gate Current will not stop conduction because already the transistor Q_2 is ON and it provides the base injection for Q_1.



$I_{B_1} = I_{c_2}$, $I_{c_1} = I_{B_2}$

Anode Current $= I_A = I_{E_1}$.

General expression for I_c interms of β, I_B & I_{co} is

$$I_c = \beta I_B + (1+\beta) I_{co}$$

Since for Transistor Q_1, $I_{c_1} = \beta_1 I_{B_1} + (1+\beta_1) I_{co1}$

since for Transistor Q_2, $I_{c_2} = \beta_2 I_{B_2} + (1+\beta_2) I_{co_2}$

But $I_{B_2} = I_{c_1}$

$$I_{c_2} = \beta_2 I_{c_1} + (1+\beta_2) I_{co_2}$$

$I_A = I_{E_1} = I_{c_1} + I_{B_1}$ But I_{c_1} is given.

$$I_A = \beta_1 I_{B_1} + (1+\beta_1) I_{CO1} + I_{B_1}$$

$$I_{E_1} = I_A = (1+\beta_1)(I_{B_1} + I_{CO1})$$

Since we must get an expression for I_{B_1}.

$$\therefore I_{C_2} = \beta_2 (\beta_1 I_{B_1} + (1+\beta_1) I_{CO1}) + (1+\beta_2) I_{CO2}$$

But $I_{C_2} = I_{B_1}$.

$$\therefore I_{B_1} = \beta_2 \beta_1 I_{B_1} + \beta_2 (1+\beta_1) I_{CO1} + (1+\beta_2) I_{CO2}$$

$$\text{or } (1-\beta_1\beta_2) I_{B_1} = \beta_2 (1+\beta_1) I_{CO1} + (1+\beta_2) I_{CO2}$$

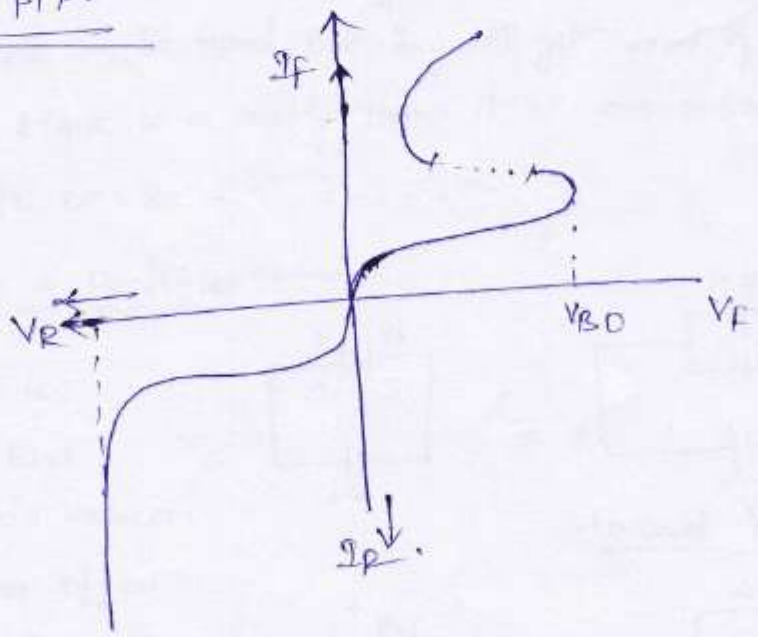
$$\text{or } I_{B_1} = \frac{\beta_2 (1+\beta_1) I_{CO1} + (1+\beta_2) I_{CO2}}{1-\beta_1\beta_2}$$

$$I_{E_1} = I_A = (1+\beta_1)\left[\frac{\beta_2(1+\beta_1) I_{CO1} + (1+\beta_2) I_{CO2} + I_{CO1}}{1-\beta_1\beta_2}\right]$$

$$= (1+\beta_1)\left[\frac{\beta_2 I_{CO1} + \beta_1\beta_2 I_{CO1} + I_{CO2} + \beta_2 I_{CO2} + I_{CO1} - \beta_1\beta_2 I_{CO1}}{1-\beta_1\beta_2}\right]$$

$$= (1+\beta_1)\left[\frac{I_{CO1}(1+\beta_2) + I_{CO2}(1+\beta_2)}{1-\beta_1\beta_2}\right]$$

$$I_{E_1} = \frac{(1+\beta_1)(1+\beta_2)(I_{CO1} + I_{CO2})}{1-\beta_1\beta_2}$$



Diode Switching Times:—

Forward Recovery Time (T_{FR}):—

→ Time taken by the diode to reach from 10% to the 90% of the applied voltage is called the "Forward Recovery Time".

Reverse Recovery Time (T_{RR}):—

→ Time taken by the diode to reach from 90% to the 10% of the applied voltage is called "Reverse Recovery Time".

Rectifier:—

Rectifier is a circuit which offers low resistance to the current in one direction and high resistance in the opposite direction.

→ Rectifier converts sinusoidal signal to unidirectional flow [i.e., AC to pulsating DC] and not pure D.C.

→ filter converts unidirectional flow into pure DC.

→ Rectifier output is not a pure D.C. To get the pure DC waveform we need to add one more device i.e., filter along with the Rectifier

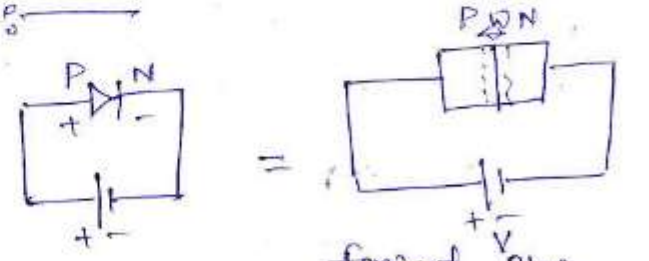
→ Rectifier + filter converts Alternating Current to pure DC.

→ Purpose of Rectification:

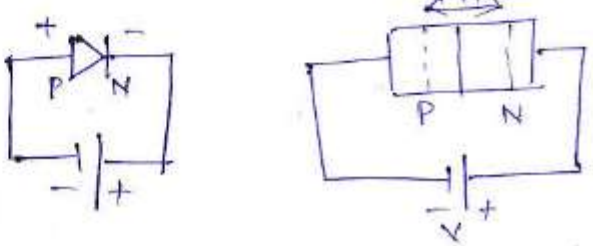
The electronic circuits require a DC source of power. for transistor A.C. amplifier circuit for biasing DC supply is required. The input signal can be AC and so the output signal will be amplified AC signal. But without Biasing with DC supply, the amp circuit will not work. So more or less all electronic AC instruments require DC power. To get this, DC batteries can be used. But they will get dried quickly and replacing them every time is a costly. Hence it is economical to convert AC power into DC.

The P-N Junction as a Rectifier:—

If PN Junction Diode is connected in forward Bias, the depletion region width reduces. Then this thin barrier offers low resistance. So maximum Current flows through the diode.



If PN Junction Diode is connected in Reverse bias, the depletion region width increases. Then this Thick barrier offers high resistance. so minimum Current flows through the diode i.e., less amount of current flows through the diode in Reverse bias.



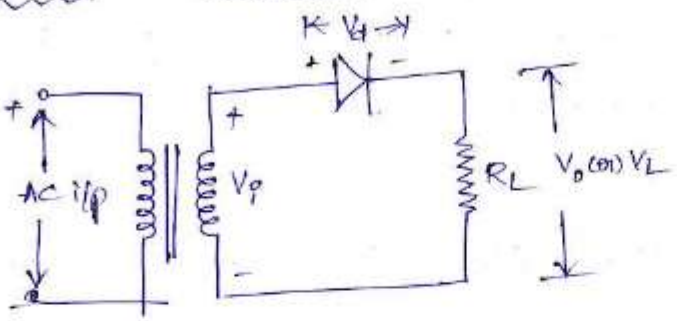
Reverse Bias

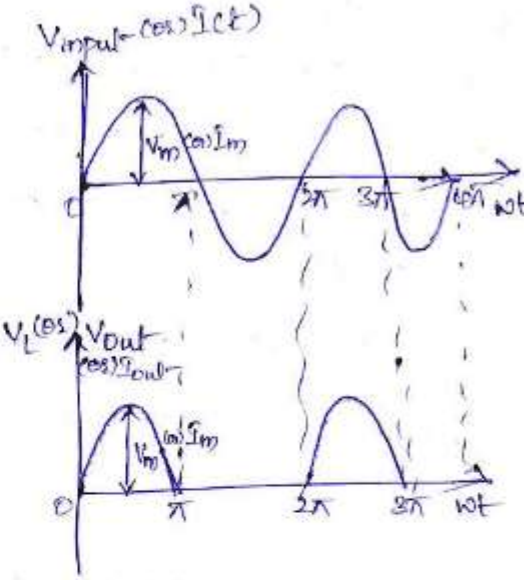
→ Diode in forward Bias offers low resistance and offers high resistance in Reverse Bias.

→ Rectifier offers low resistance to the current in one direction and high resistance in the opposite direction.

∴ So Diode can also acts as a Rectifier.

Half Wave Rectifier :





The input signal for the rectifier is

$v(t) = V_i = V_m \sin\omega t$, $0 \le \omega t \le 2\pi$

(or)

$i(t) = I_m \sin\omega t$, $0 \le \omega t \le 2\pi$

If the input signal for the rectifier circuit is $V_i = V_m \sin\omega t$, has a peak value V_m, which is very large compared with the cut-in voltage 'V_γ' of the diode. Assume the diode cut-in voltage is $V_\gamma = 0$ i.e, we consider an ideal diode.

With the diode idealized to be a resistance R_f in the ON state and an open circuit in the OFF state. The current $i(t)$ & voltage v_{out} at load R_L is given by

i_{out} (or) $i = I_m \sin\omega t$, $0 \le \omega t \le \pi$

$= 0$, $\pi \le \omega t \le 2\pi$

V_{out} (or) $V_L = V_m \sin\omega t$, $0 \le \omega t \le \pi$

$= 0$, $\pi \le \omega t \le 2\pi$

Here $I_m = \dfrac{V_m}{R_f + R_L}$

→ From the observations, the output of Half wave Rectifier is unidirectional.

→ We can calculate this non zero value of the average current by a DC meter.

(i) Reading of DC Ammeter :—

DC Ammeter is constructed such that to calculate or measure the average value. In this meter, the deflection of needle shows the average value of the current passing through it.

DC voltage or (Ammeter) Current — can be calculated by the area of one cycle of the curve divided by the base.

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i(t)\,d\omega t$$ → Gives the average value of any waveform

Since $i(t) = I_m \sin\omega t, \quad 0 \le \omega t \le \pi$

$= 0, \quad \pi \le \omega t \le 2\pi$

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t\,d\omega t = \frac{I_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$= -\frac{I_m}{2\pi}\left[\cos\pi - \cos 0\right] = -\frac{I_m}{2\pi}\left[-1-1\right] = \frac{I_m}{2\pi}(+2)$$

**

$$I_{dc} = \frac{I_m}{\pi}$$ → Half wave Rectifier.

(ii) Reading of AC Ammeter :—

An AC Ammeter is constructed to measure the effectiveness or rms value ~~separated~~ of a Rectifier output. In this Ammeter, the deflection of needle shows the RMS current passing through it.

→ The effectiveness or I_{rms} rms value squared of a periodic function of a time is given by the area of one cycle of the curve, which represents square of the function, divided by the base.

Mathematically,

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2(t)\,d\omega t}$$

RMS of o/p is

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_0^2(t)\,d\omega t} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}(I_m\sin\omega t)^2\,d\omega t} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}\sin^2\omega t\,d\omega t}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d\omega t} = \sqrt{\frac{I_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}} = \sqrt{\frac{I_m^2}{4\pi}\left[\pi\right]}$$

**

$$I_{rms} = \frac{I_m}{2}$$ → Half wave Rectifier

(iii) Diode voltage:—

The dc output voltage is given as

$$V_{dc} = I_{dc} R_L = \frac{I_m R_L}{\pi}$$

However, the reading of a dc voltmeter placed across the diode is not given by $I_{dc} R_f$ because diode cannot be modeled as a constant resistance but rather it has two values: R_f is ON state & ∞ in the off state.

A dc voltmeter reads the average value of the voltage across its terminals. Hence to obtain V_{dc}' across the diode instantaneous voltage must be plotted and average value obtained by Integration

Thus
$$V_{dc}' = \frac{1}{2\pi}\left(\int_0^{\pi} I_m R_f \sin\omega t\, d\omega t + \int_{\pi}^{2\pi} V_m \sin\omega t\, d\omega t\right)$$

$$= \frac{1}{2\pi}\left(I_m R_f \left[-\cos\omega t\right]_0^{\pi} + V_m \left[-\cos\omega t\right]_{\pi}^{2\pi}\right)$$

$$= \frac{1}{2\pi}\left[-I_m R_f (-2) - V_m (1+1)\right] = \frac{1}{\pi}\left[I_m R_f - V_m\right]$$

where $V_m = I_m (R_f + R_L)$

$$V_{dc}' = \frac{1}{\pi}\left[I_m R_f - I_m R_f - I_m R_L\right] = \frac{-I_m R_L}{\pi}$$

$$V_{dc}' = \frac{-I_m R_L}{\pi}, \quad \text{where } I_m = \frac{V_m}{R_f + R_L}$$

Here negative indicates that the voltmeter is connected to the diode with positive of Battery is connected to Anode and negative of Battery is connected to the Cathode of the Battery or meter. In order to overcome this, we must connect +ve of meter is connected to cathode and -ve of meter is connected to the Anode.

→ The dc voltage across diode is seen to be equal to the negative of the dc voltage across the load resistor.

(iv) Reading of Wattmeter:—

This meter is to indicate the average value of the product of the instantaneous current through its coil and the instantaneous voltage across its potential coil.

$$P_i = \frac{1}{2\pi}\int_0^{2\pi} V_p i\, d\omega t \quad \text{since } V_i = i(R_f + R_L) \quad 0 \le \omega t \le \pi$$

$$= \frac{1}{2\pi}\int_0^{\pi} i^2 (R_f + R_L)\, d\omega t = \frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t\,(R_f + R_L)\, d\omega t$$

$$\boxed{P_i = I_{rms}^2 (R_f + R_L)}$$

Regulation:

The variation of dc o/p voltage as a function of dc load current is called "Regulation".

$$\% \text{ Regulation} = \frac{V_{NoLoad} - V_{full\ Load}}{V_{full\ Load}} \times 100\ \%$$

→ For an ideal power supply the output voltage is independent of the load and percentage regulation is zero.

→ The variation of V_{dc} with I_{dc} for the Half wave Rectifier is obtained as follows:

$$I_{dc} = I_m/\pi \quad \text{where} \quad I_m = \frac{V_m}{R_f + R_L}$$

$$\therefore I_{dc} = \frac{V_m}{\pi(R_f + R_L)}$$

$$V_{dc} = I_{dc} R_L$$

$$V_{dc} = \frac{V_m}{\pi(R_f+R_L)}(R_f + R_L - R_f) = \frac{V_m}{\pi}\left(1 - \frac{R_f}{\pi(R_f+R_L)}\right) = \frac{V_m}{\pi} - \frac{V_m R_f}{\pi(R_f+R_L)}$$

$$\therefore \boxed{V_{dc} = \frac{V_m}{\pi} - I_{dc} R_f}$$

V_{NoLoad} means voltage across the load terminals when load current passes is zero [i.e. $I_{dc}=0$].

$V_{Full\ Load}$ means voltage across the load terminals when load current is Max.

$$V_{NoLoad} = \frac{V_m}{\pi}, \quad V_{full\ load} = \frac{V_m}{\pi} - I_{dc} R_f$$

$$\therefore \% \text{ Regulation} = \frac{\frac{V_m}{\pi} - \frac{V_m}{\pi} + I_{dc} R_f}{\frac{V_m}{\pi} - I_{dc} R_f} \times 100$$

$$= \frac{I_{dc} R_f}{I_{dc} R_f \left[\frac{V_m}{\pi I_{dc} R_f} - 1\right]} \times 100 = \frac{1}{\frac{V_m}{\pi} \times \frac{\pi(R_f+R_L)}{V_m} - 1} \times 100$$

$$\% \text{ Regulation} = \frac{1}{\frac{R_f+R_L}{R_f} - 1} \times 100 = \frac{R_f}{R_f + R_L - R_f} \times 100$$

$$\boxed{\% \text{ Regulation} = \frac{R_f}{R_L} \times 100}$$

Ripple factor:- ——— (γ)

→ A measure of the fluctuating components is given by "Ripple factor".

$$\gamma = \frac{\text{rms Value of Alternating component of Wave}}{\text{Average Value of Wave}}$$

$$\gamma = \frac{I'_{rms}}{I_{dc}} = \frac{V'_{rms}}{V_{dc}}$$

→ Ripple factor should be small.

→ We should derive the expression for the ripple factor. The instantaneous current is given by

$$I_{AC} = i - I_{dc}$$

rms of AC, $I'_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(I - I_{dc})^2 d\omega t}$

$$I'_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(I^2 - 2I_{dc}I + I_{dc}^2)d\omega t}$$

$\frac{1}{2\pi}\int_0^{2\pi} i^2 d\omega t$ = Square of the rms Value of a Sine wave

$= (I_{rms})^2$

$\frac{1}{2\pi}\int_0^{2\pi} i\, d\omega t$ = The Average Value (or) DC Value I_{DC}

I_{DC} is constant.

$$\therefore I'_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I^2 d\omega t - 2I_{dc}\cdot\frac{1}{2\pi}\int_0^{2\pi} I\, d\omega t + \frac{I_{dc}^2}{2\pi}\int_0^{2\pi} d\omega t}$$

$$= \sqrt{I_{rms}^2 - 2I_{dc}^2 + \frac{I_{dc}^2}{2\pi}(2\pi)} = \sqrt{(I_{rms})^2 - 2I_{dc}^2 + I_{dc}^2}$$

$$I'_{rms} = \sqrt{(I_{rms})^2 - I_{dc}^2}$$

$$\text{ripple factor} = \frac{I'_{rms}}{I_{dc}}$$

$$= \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\therefore \boxed{\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}} \rightarrow \text{General formulae for the Rectifiers.}$$

for Half Wave Rectifier:

$$I_{dc} = \frac{I_m}{\pi}, \quad I_{rms} = \frac{I_m}{2}$$

$$\therefore r = \sqrt{\frac{(I_m/2)^2}{(I_m/\pi)^2} - 1} = \sqrt{\frac{I_m^2 \times \pi^2}{I_m^2 \times 4} - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$r = 1.21$$

This results indicates that the rms ripple voltage exceeds the dc o/p voltage and shows that the HWR is relatively poor circuit for converting AC into DC.

Ratio of Rectification! — (η):

This gives the amount of AC input signal is being converted into DC.

Ratio of Rectification (η) = $\frac{\text{DC power delivered to the load}}{\text{AC input power from transformer secondary}}$

$$\eta = \frac{P_{DC}}{P_{AC}}$$

Here $P_{DC} = I_{dc}^2 R_L$ But $I_{dc} = \frac{I_m}{\pi}$

$$\therefore P_{DC} = \frac{I_m^2}{\pi^2} R_L$$

P_{AC} is the what the wattmeter would indicate if placed in the HWR circuit with its voltage terminals connected across the secondary of the transformer.

from π to 2π, the diode is non-conducting. Hence $I_{ac} = 0$ in π to 2π.

$$\therefore P_{ac} = (I_{rms})^2 (R_f + R_L)$$

for the HWR, $I_{rms} = \frac{I_m}{2}$.

$$\therefore P_{ac} = \frac{I_m^2}{4}(R_f + R_L)$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{I_m^2/\pi^2 R_L}{\frac{I_m^2}{4}(R_f + R_L)} = \frac{4}{\pi^2} \cdot \frac{R_L}{R_f + R_L} = \frac{4}{\pi^2} \cdot \frac{1}{1 + \frac{R_f}{R_L}}$$

$$\therefore \boxed{\eta = \frac{0.406}{1 + \frac{R_f}{R_L}}}$$ This is applicable even for practical diode,

for an ideal diode, $R_f = 0$

$\eta = 0.406$ → only 40.6% of the i/p Ac is converted into Dc.

→ part of the Ac input power is converted into DC and remaining is dissipated in the load.

Transformer Utilization factor (TUF):—

→ It indicates the amount of the utilization of the transformer in the circuit.

→ TUF is defined as the ratio of dc power delivered to the load to the Ac power rating of the transformer. While calculating the Ac power rating it is necessary to consider rms value of Ac voltage or Current.

Ac power rating of Transformer $= V_{rms} \cdot I_{rms}$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2} = \frac{V_m I_m}{2\sqrt{2}}$$

Remember that the secondary voltage is purely sinusoidal hence its rms value is $\frac{1}{\sqrt{2}}$ times maximum. while the current is half sinusoidal hence its rms value is $\frac{1}{2}$ of the maximum.

DC power delivered to the load $= P_{dc} = I_{dc}^2 R_L = (I_m/\pi)^2 R_L$.

$$TUF = \frac{(I_m/\pi)^2 R_L}{\frac{V_m I_m}{2\sqrt{2}}} \quad \text{Here } V_m = I_m[R_L + R_f]$$

$$TUF = \frac{I_m^2 \times R_L \times 2\sqrt{2}}{\pi^2 I_m^2 \times [R_f + R_L]} = \frac{2\sqrt{2}}{\pi^2} \frac{R_L}{R_f + R_L} = \frac{2\sqrt{2}}{\pi^2} \cdot \frac{1}{1 + R_f/R_L}$$

$$\boxed{TUF = 0.287 \frac{1}{1 + R_f/R_L}}$$ → Applicable for practical also.

for ideal diodes, $R_f = 0$. R_f → forward Resistance of diode

$$\therefore \boxed{TUF = 0.287}$$

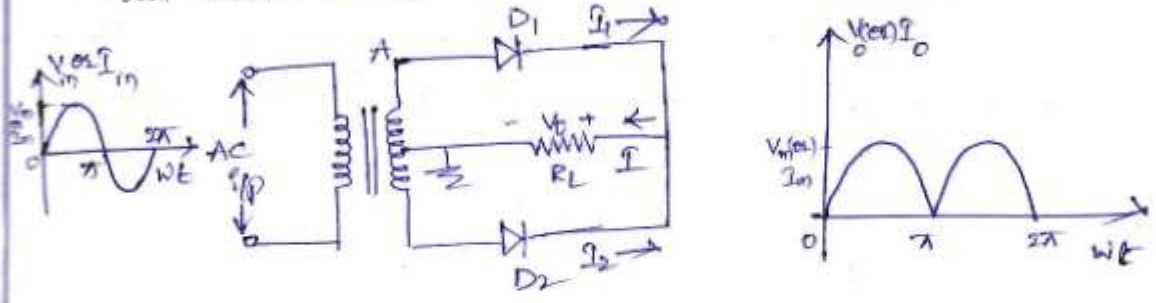
The value of TUF is low, which shows that in Half wave circuit, the transformer is not fully utilized.

Disadvantages of HWR:—

→ High ripple factor [1.21]
→ Low ratio of rectification (0.406)
→ Low Transformer utilization factor (TUF).
→ Because of ripple voltage exceeds D.C. Voltage, HWR is a poor circuit for converting AC to DC.

Full Wave Rectifier (FWR):—

→ To increase the ripple factor in Half Wave Rectifier we use full Wave Rectifier.

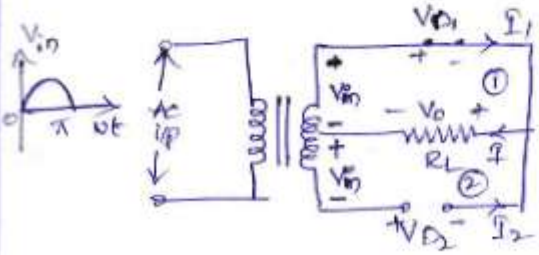


Operation:—

During the positive Half cycle

This circuit is seen to comprise two half Wave Circuits which are connected that conduction takes place through one diode during one half of the power cycle and through the other diode during the second half of the power cycle.

During the positive half cycle, D_1 conducts and D_2 not conducts. so the current flows through the diode D_2 is zero.



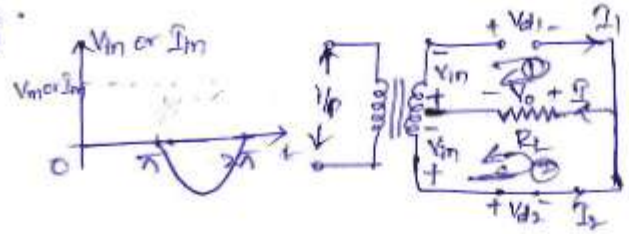
from Loop ①, By KVL.

$V_m - V_{D1} - V_o = 0$ where $V_{D1} = 0$

$\therefore \boxed{V_o = V_m}$

In the positive half cycle, the voltage across load resistor as output voltage is same as the input applied to the Rectifier.

During the negative half cycle, D_2 conducts and the D_1 non-conducts. So the current passes through D_1 is zero and the total current passes through D_2 only.



$I_1 = 0$, $I = I_1 + I_2$

$\boxed{I = I_2}$ → (9)

By KVL from Loop ①,

$-V_{in} - V_{d1} - V_o = 0$.

$V_o = -V_{in} - V_{d1}$ → (1)

from eqn (1), Here $V_o = 0$.

$-V_{in} - V_{d1} = 0$.

$\boxed{V_{d1} = -V_{in}}$

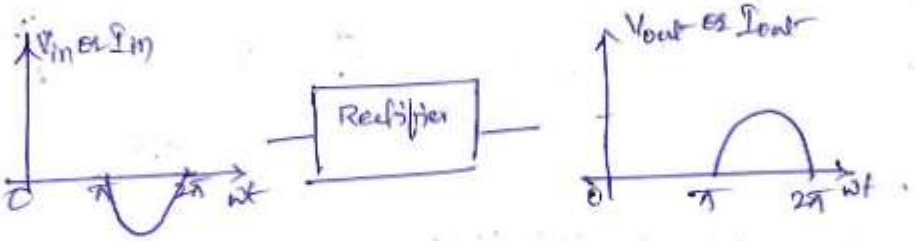
But from loop ②, ($\because V_{d2} = 0$)

$-V_{d2} + V_{in} - V_o = 0 \Rightarrow V_{in} = V_o$ → (2)

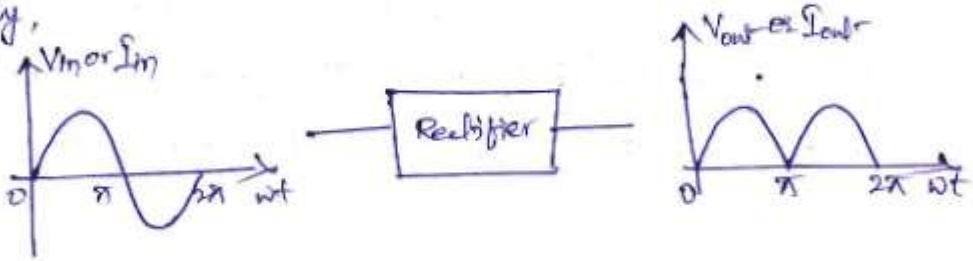
from (1) & (2), $V_{d1} = -V_{in} - V_o = -2V_{in} = -2V_o$

→ condition (9) is not correct because current always flows from positive to negative. But from the current leaving at +ve of V_{in}.

so $I = -I_2$. therefore $V_o = -V_{in}$ in negative half cycle.



finally,



for a full wave Rectifier,

$V_o^{(t)}$ or $V_L = V_{in}$, → $V_o^{(t)}$ or $V_L = V_m \sin\omega t$, $0 \le \omega t \le \pi$

$V_o^{(t)}$ or $V_L = -V_{in}$, → $V_o^{(t)}$ or $V_L = -V_m \sin\omega t$, $\pi \le \omega t \le 2\pi$.

→ The current to the load is the sum of dc and rms values of the load current.

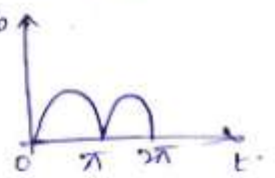
→ A centre tapped transformer is essential to get full wave rectification. So there is a phase shift of 180°, because of centre tapping.

→ $I_o^{(t)} = I_m \sin\omega t = I_m^{(t)}$, $0 \le \omega t \le \pi$

$= -I_m \sin\omega t = -I_{in}^{(t)}$, $\pi \le \omega t \le 2\pi$

case(i):— DC Current—

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I_0(t)\,d\omega t = \frac{1}{2\pi}\left[\int_0^{\pi} I_0(t)\,d\omega t + \int_{\pi}^{2\pi} I_0(t)\,d\omega t\right]$$



$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t\,d\omega t + \int_{\pi}^{2\pi} -I_m \sin\omega t\,d\omega t\right]$$

$$= \frac{I_m}{2\pi}\left[(-\cos\omega t)_0^{\pi} + (-\cos\omega t)_{\pi}^{2\pi}\right] = \frac{I_m}{2\pi}\left[1+1+1+1\right] = \frac{I_m}{2\pi}[4]$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

case(ii):— RMS Current of FWR

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_0^2(t)\,d\omega t} = \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_0(t)\,d\omega t + \int_{\pi}^{2\pi} I_0(t)\,d\omega t\right]}$$

$$= \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} (I_m \sin\omega t)^2\,d\omega t + \int_{\pi}^{2\pi} (-I_m \sin\omega t)^2\,d\omega t\right]}$$

$$= \sqrt{\frac{1}{2\pi}\cdot I_m^2\left[\int_0^{\pi} \sin^2\omega t\,d\omega t + \int_{\pi}^{2\pi} \sin^2\omega t\,d\omega t\right]} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{2\pi} \sin^2\omega t\,d\omega t}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{2\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d\omega t} = \sqrt{\frac{I_m^2}{4\pi}\int_0^{2\pi}\left[1-\cos 2\omega t\right]d\omega t}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{2\pi}} = \sqrt{\frac{I_m^2}{4\pi}\left[2\pi - 0\right]} = \sqrt{\frac{I_m^2}{2}}$$

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

case(iii):— Ripple factor (r):

$$r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}, \quad I_{dc} = \frac{2I_m}{\pi}$$

$$\therefore r = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{I_m^2 \times \pi^2}{2 \times 4I_m^2} - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

from this 48.2% of the wave having ripples.

case(iv):- Regulation:-

$$\% \text{ Regulation} = \frac{V_{No\,load} - V_{full\,load}}{V_{full\,load}} \times 100$$

Since $V_{dc} = I_{dc} R_L$

$$= \frac{2I_m}{\pi} R_L = \frac{2V_m}{\pi(R_f+R_L)} R_L = \frac{2V_m (R_f+R_L-R_f)}{\pi(R_f+R_L)}$$

$$V_{dc} = \frac{2V_m}{\pi} - \frac{2V_m R_f}{\pi(R_f+R_L)} = \frac{2V_m}{\pi} - I_{dc} R_f$$

$$\therefore \boxed{V_{dc} = \frac{2V_m}{\pi} - I_{dc} R_f}$$

$$V_{noload} = \frac{2V_m}{\pi} \quad [\text{i.e., } I_{dc} = 0]$$

$$V_{full\,load} = \frac{2V_m}{\pi} - I_{dc} R_f$$

$$\% \text{ Regulation} = \frac{\frac{2V_m}{\pi} - \frac{2V_m}{\pi} + I_{dc} R_f}{\frac{2V_m}{\pi} - I_{dc} R_f} \times 100$$

$$= \frac{1}{\frac{2V_m}{\pi(I_{dc} R_f)} - 1} \times 100 = \frac{1}{\frac{2V_m[\pi(R_f+R_L)]}{\pi \cdot 2V_m R_f} - 1} \times 100$$

$$= \frac{1}{\frac{R_f+R_L}{R_f} - 1} \times 100 = \frac{1}{\frac{R_f+R_L-R_f}{R_f}} \times 100 = \frac{R_f}{R_L} \times 100$$

$$\boxed{\% \text{ Regulation} = \frac{R_f}{R_L} \times 100}$$

case(v):- Ratio of Rectification (η):-

$$\eta = \frac{P_{DC}}{P_{AC}}$$

where $P_{DC} = I_{DC}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L = \frac{4I_m^2}{\pi^2} R_L$

$$P_{AC} = I_{rms}^2 (R_f+R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f+R_L) = \frac{I_m^2}{2}(R_f+R_L)$$

$$\therefore \eta = \frac{P_{DC}}{P_{AC}} = \frac{\frac{4I_m^2 R_L}{\pi^2}}{\frac{I_m^2}{2}(R_f+R_L)} = \frac{4I_m^2 R_L * 2}{\pi^2 I_m^2 (R_f+R_L)} = \frac{8}{\pi^2} \frac{R_L}{R_f+R_L} = \frac{8}{\pi^2} \cdot \frac{1}{1+\frac{R_f}{R_L}}$$

$$\eta = 0.811 \frac{1}{1+R_f/R_L}$$

$$\eta = 0.811 * \frac{1}{1+\frac{R_f}{R_L}}$$

case(vi):-

Transformer utilization factor (TUF):-

In full wave Rectifier using center tapped transformer the secondary current flows through each half separately in every half cycle. while the primary of transformer carries current continuously. Hence TUF is called calculated for primary and secondary windings separately and then the average TUF is determined.

$$\text{Secondary TUF} = \frac{\text{DC power delivered to load}}{\text{Ac rating of Transformer secondary}}$$

$$= \frac{(I_{DC})^2 R_L}{V_{rms} I_{rms}} = \frac{(2I_m/\pi)^2 \cdot R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{8 I_m^2 R_L}{\pi^2 V_m I_m}$$

$$= \frac{8 I_m R_L}{\pi^2 V_m} \qquad \because V_m = I_m(R_f + R_L)$$

$$= \frac{8 I_m R_L}{\pi^2 I_m (R_f + R_L)} = \frac{8}{\pi^2} \cdot \frac{R_L}{R_f + R_L} = \frac{8}{\pi^2} \cdot \frac{1}{1+\frac{R_f}{R_L}}$$

$$TUF = 0.812 \frac{1}{1+R_f/R_L}$$

The primary of the transformer in feeding two Half Wave Rectifiers separately. these two Half Wave Rectifiers work independently of each other but feed a common load. Therefore

$$\text{TUF for primary} = 2 \times \text{TUF of HWR}$$

$$= 2 \times \frac{0.287}{1+R_f/R_L} = \frac{0.574}{1+R_f/R_L}$$

The average TUF for FWR using center tapped transformer is

$$= \frac{\text{TUF of psimary} + \text{TUF of secondary}}{2}$$

$$= \frac{0.812 + 0.574}{2} = 0.693$$

Therefore, the transformer is utilized 69.3%. in full wave Rectifier using center tapped transformer.

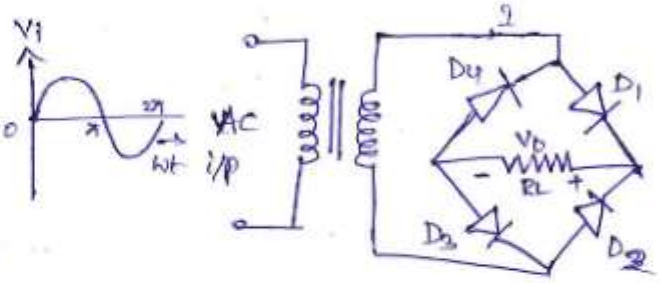
cont(vii):

Peak Inverse Voltage:-

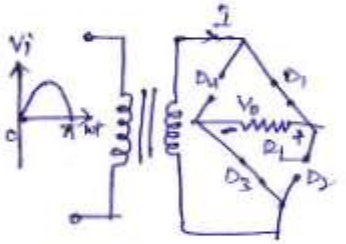
During the negative half cycle, D_1 is not conducting and D_2 is conducting. Hence Maximum Voltage across R_L is V_m Since Voltage is also present between the transformer. The total Voltage across diode D_1 is $V_m + V_m = 2V_m$.

Bridge Rectifier:-

→ Bridge Rectifier is a type of full Wave Rectifier. The circuit of Bridge Rectifier as shown below.

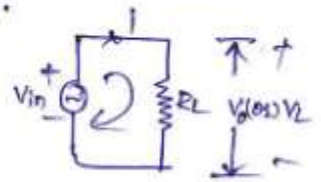


→ When the input for the Bridge Rectifier is positive half cycle, then the diodes D_1 and D_3 are in fowward Bias and D_2 and D_4 are in Reverse Bias. So D_1 and D_3 are become shorted and D_2 and D_4 becomes open circuited. Then the Current from the input is passes to the Load. Whatever the Voltage is applied at the input that is appeared across the load.



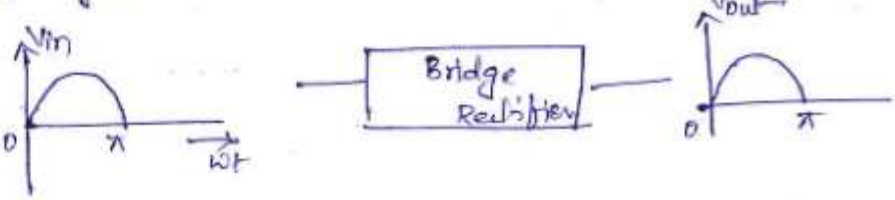
ckt diagram for +Ve half cycle

By KVL, $V_{in} - V_o = 0 \Rightarrow \boxed{V_o = V_{in}}$



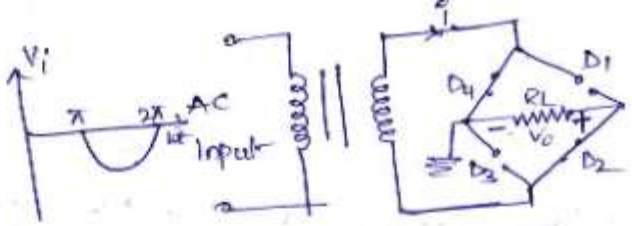
∴ The output of the Rectifier is same as the input applied for the positive half cycle.

→



→ If the input for the Bridge rectifier is negative half cycle, then the diodes D_1 and D_3 are in Reverse Bias and D_2 and D_4 are in fowward Bias. So D_1 and D_3 diodes becomes open and diodes D_2 and D_4 becomes shorted. Then the Current from the input is passes to the load.

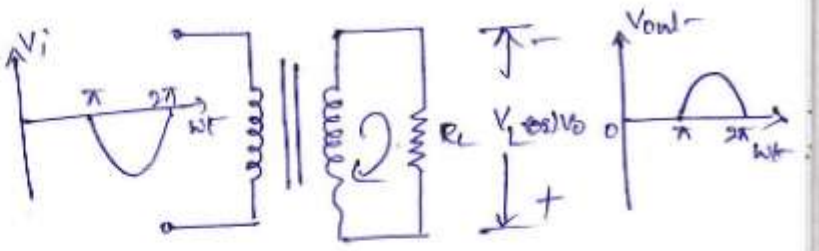
→ Whatever the voltage is applied, that the negative of the input is appeared across the load.

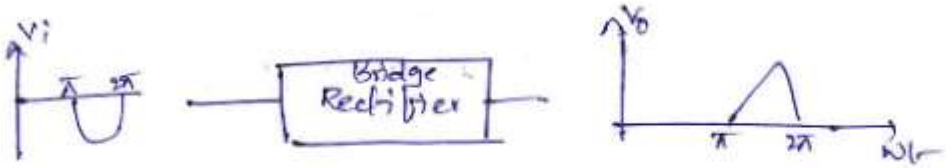


By KVL,

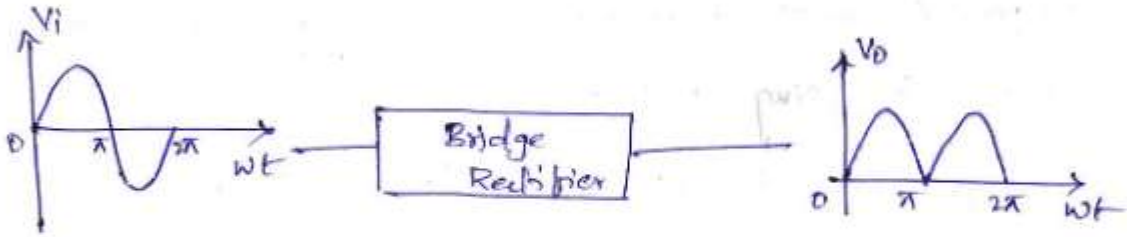
$+V_i + V_o = 0$

$V_o = -V_{in}$





*)



Advantages:-

→ peak Inverse voltage is V_m only.

→ centre tapped transformer is not required.

→ There is no DC Current flows through the transformer. Transformer utilization factor increases.

Disadvantages:-

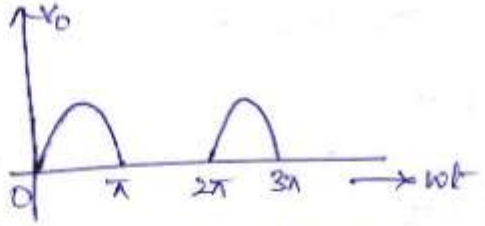
→ In this we use four diodes, so voltage drop across all diodes must be considered.

contd):

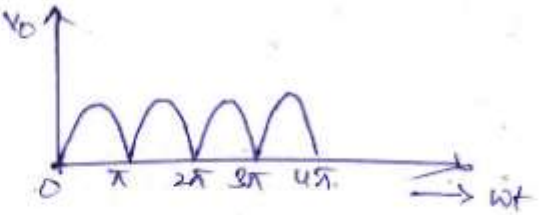
The Harmonic Components in Rectifier Circuits:

→ The output voltage from a rectifier is not pure DC.

The output voltage from the ^{HW} Rectifier is



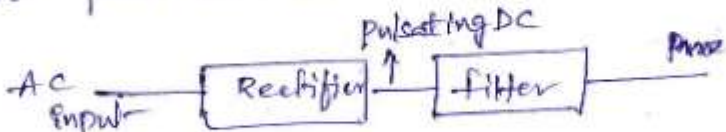
The output voltage from the full wave Rectifier is



These waveforms are not in pure DC i.e., these are having some ripple components in the output. These ripples can be removed or reduced by using filters.

→ The Rectifier converts AC to pulsating DC.

→ filter removes or reduces harmonics, i.e. it converts pulsating DC into pure DC. So Rectifier and filter gives pure DC.



→ Sometimes filter output also contains small amount of AC components. These AC components [even and odd harmonics] can be calculated by using fourier series analysis i.e., By using fourier series, analytical representation of the output current wave in a rectifier is obtained.

The result of such analysis for the Half wave Rectifier circuit leads to the following expression for the current waveform.

$$I = I_m\left[\underbrace{\frac{1}{\pi}}_{\text{dc component}} + \underbrace{\frac{1}{2}\sin\omega t}_{\text{odd harmonic}} - \frac{2}{\pi}\sum_{\substack{K=\text{even} \\ (\neq 0)}} \frac{\cos K\omega t}{(K+1)(K-1)}\right]$$

Even harmonics

The lowest angular frequency present in this expression is that of the

The full wave Rectifier Circuit consists of two half wave rectifier circuits which are arranged that one circuit conducts during one half cycle and the second operates during the second half cycle. It is clear that the currents are functionally related by the expression $i_1(\omega t) = i_2(\omega t + \pi)$. The total load current $i = i_1 + i_2$ attains the form

$$I = I_m\left[\underbrace{\frac{2}{\pi}}_{\text{DC term}} - \underbrace{\frac{4}{\pi}\sum_{k=\text{even}} \frac{\cos k\omega t}{(k+1)(k-1)}}_{\text{Even Harmonics } (\neq 0)}\right]$$

→ The output of HWR consists of DC component along with AC components. In AC components both even and odd harmonic components are present.

→ Because of phase shift introduced, odd harmonics in the full wave rectifier removed only even harmonics are present in the ~~filter~~ Rectifier output.

Inductance filter :—

→ The property of inductor is, it does not allows sudden change of current in the circuit. Incase of AC, there is change in the Magnitude of current with time.

→ Inductor acts as short circuit for DC and offers some impedance for AC. so it can be used as a filter.

AC voltage is dropped across the inductor where as DC passes through it. Therefore AC minimized in the O/p.

$Z_L = X_L = j\omega L$
$= j2\pi f L$

$f = 0 \Rightarrow DC \Rightarrow Z_L = 0$
L = Short

as $f \uparrow \rightarrow Z_L \rightarrow \uparrow$.

at $f = 0 \Rightarrow Z_L = 0$
L → open

→ According to fourier Analysis, Current I in the Half Wave Rectifier Circuit is

$$I = \frac{I_m}{\pi} + \frac{I_m}{2}\sin\omega t - \frac{2I_m}{\pi}\frac{\cos 2\omega t}{3}$$

Current in the case of full wave Rectifier is

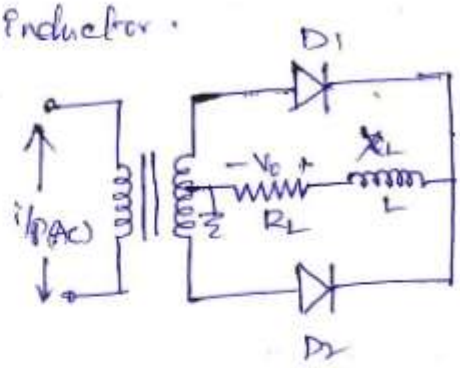
$$I = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t - \frac{4I_m \cos 4\omega t}{15\pi} - \frac{4I_m \cos 6\omega t}{35\pi} \ldots$$

The reactance offered by inductor to higher order frequencies like 4ωt, 8ωt etc can be neglected. so the output current is.

since $Z_L = j2\pi f L = Z_L = j\omega L$
as $\omega \uparrow \Rightarrow Z_L \uparrow$

$$i = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t$$

The fundamental harmonic frequency 'ω' is eliminated. one winding of Transformer can be used as inductor.



→ for simplification, diode and choke (Inductor) resistances can be neglected compared with R_L. Hence the DC component of the current is

$$i_m = \frac{V_m}{Z_L} \quad \text{where } Z_L = |R_L + jX_L| = \sqrt{R_L^2 + X_L^2}$$

for the second harmonic the frequency is 2ω.

$$\therefore Z_L = \sqrt{R_L^2 + (2\omega L)^2} = \sqrt{R_L^2 + 4\omega^2 L^2}$$

Therefore AC component of current

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}.$$

By substituting these values in the expression for current

$$i = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t.$$

By inductor to higher order frequencies like 4ωt, 6ωt &c. we get

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}}\cos(2\omega t - \theta)$$

where 'θ' is the angle by which the load current lags behind the voltage and is given by

$$\boxed{\theta = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)}$$

RDC
II (10)

Ripple factor :-

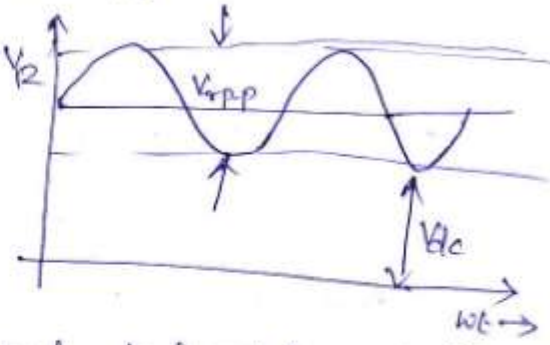
$$r = \frac{I_{rms}}{I_{DC}} \qquad I_{DC} = \frac{2V_m}{\pi R_L}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L + 4\omega^2 L^2}}$$

$$r = \frac{4V_m * \pi R_L}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2} * 2V_m} = \frac{2}{3\sqrt{2}} * \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If $\frac{4\omega^2 L^2}{R_L^2} >> 1$, then $r = \frac{R_L * 2}{3\sqrt{2} * 2\omega L}$

$$\boxed{r = \frac{R_L}{3\sqrt{2}\omega L}}$$



Therefore for higher values of L, the ripple factor is low. If R_L is very large then ripple factor also high. Hence Inductor filter should be used where the value of R_L is low. Suppose the output waveform from the FWR is shown in figure then V_{rpp} is the peak-peak value of the ripple voltage.

→ If the load resistance is infinite then

$$r = \frac{2}{3\sqrt{2}} \frac{1}{\sqrt{HO}} = \frac{2}{3\sqrt{2}}$$

$$\boxed{r = 0.471}$$

Regulation :-

$$V_{dc} = I_{dc} R_L, \quad I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi(R_f + R_L)}$$

$$V_{dc} = \frac{2V_m R_L}{\pi(R_f + R_L)}$$

$$\boxed{V_{DC} = \frac{2V_m}{\pi} - I_{DC} R_f}$$

$$\% R = \frac{V_{noload} - V_{full\ load}}{V_{full\ load}} \times 100 = \frac{\frac{2V_m}{\pi} - \frac{2V_m}{\pi} + I_{DC}R_f}{\frac{2V_m}{\pi} - I_{DC}R_f} \times 100 = \frac{1}{\frac{2V_m}{\pi I_{DC} R_f} - 1} \times 100 = \frac{1}{\frac{2V_m(R_f + R_L)\pi}{\pi R_f * 2V_m} - 1} \times 100$$

$$= \frac{1}{\frac{R_L}{R_f}} \times 100 = \frac{R_f}{R_L} \times 100$$

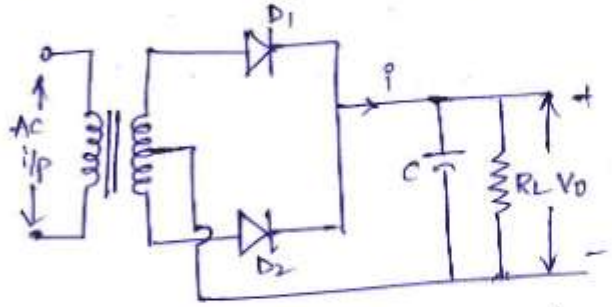
In Inductance filter the ripple factor is appsoximately 47%. i.e. appsoximately equal to the ripple factor for the full wave Rectifier.

By adding an inductance there is a small impsovement in ripple factor but the cost increases due to the inductance and it is Bulky.

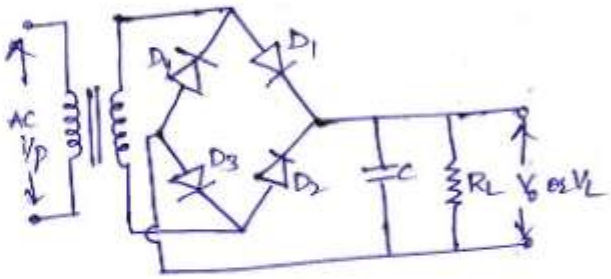
Capacitance filter:-

To improve the Ripple factor we go for the capacitance filter.

→ An inexpensive filter for high loads is found in the capacitor filter which is connected directly across the load.



Using full wave Rectifier



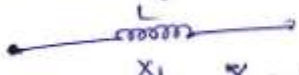
Using Bridge wave Rectifier

→ Inductors allows DC signal and blocks high (frequency) harmonic AC signals. i.e. Inductor acts as short circuit for DC and open circuit for AC signals.

→ Capacitor allows AC signals and blocks DC signals i.e. capacitor acts as open circuit for DC and short circuit for AC signals.

→ The operation of a capacitor filter is to short the ripple to ground but leave the dc to appear at the output when it is connected across a pulsating DC voltage.

→ for DC signal $f=0$.



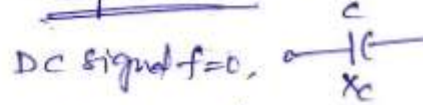
$X_L = \omega L = 2\pi f L$

for DC, $X_L = 0 \quad \because f=0$

Inductive Reactance

for DC, inductance offers zero resistance. impedance of inductor offers some impedance for AC.

→ Capacitor:-



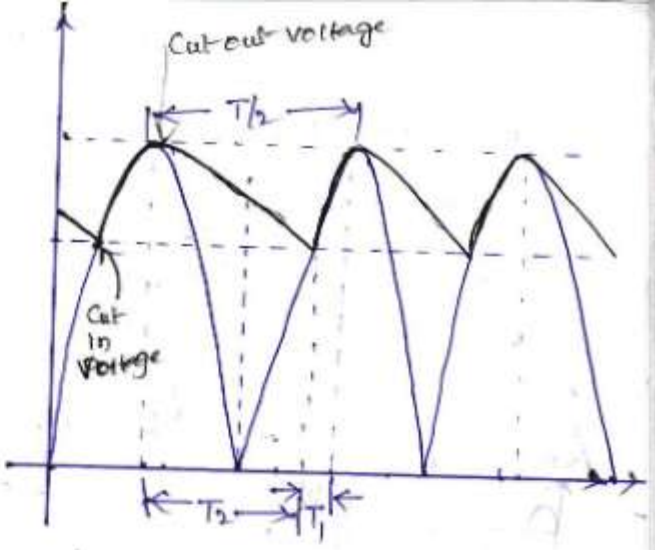
DC signal $f=0$,

$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$

for DC, $X_C = \infty \quad \because f=0$

for DC, capacitor offers high impedance i.e. ∞ and offers low impedance for AC signals.

The operation of a capacitor filter is to short the ripple to ground but leave the DC to appear at the output when it is connected across a pulsating DC voltage.



→ The diode conducts for a period which depends on the capacitor voltage. The diode will conduct when the transformer secondary voltage becomes more than the diode voltage. This is called the "cut in voltage". After this the diode stops conducting when the transformer voltage becomes less than the diode voltage. This is called the "cut-out voltage".

The charge acquired by the capacitor is

$$= V_{r\,p-p} \times C$$

$$[\, Q = CV \,]$$

The charge leaked by the capacitor is

$$= I_{dc} \times T_2$$

If the value of capacitance is large or load resistance is large then it can be assumed that the time T_2 is equal to the periodic time of the waveform.

i.e., $T_2 = T_1 = \frac{1}{2f}$ then $V_{r\,p-p} = \frac{I_{dc}}{2fc}$

$$V_{r,rms} = \frac{V_{r,p-p}}{2\sqrt{3}}$$

$$\therefore V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fc} \qquad \text{since } I_{dc} = \frac{V_{dc}}{R_L}$$

$$\therefore V_{r,rms} = \frac{V_{dc}}{4\sqrt{3}fcR_L}$$

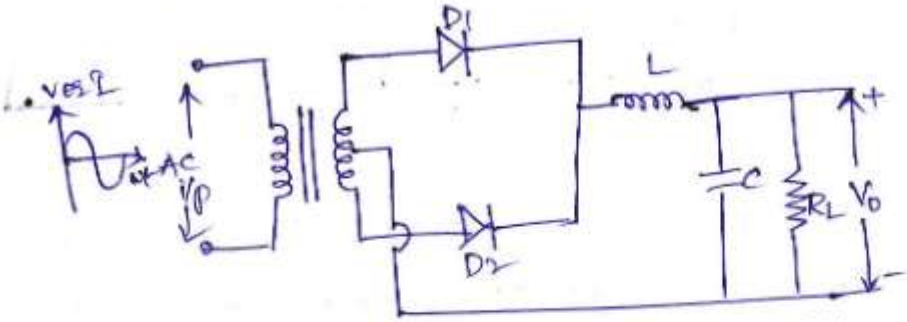
Since ripple factor $(\gamma) = \frac{V_{r,rms}}{V_{dc}}$

$$\boxed{\gamma = \frac{1}{4\sqrt{3}\,fcR_L}}$$

The ripple may be decreased by increasing 'c' or 'R_L' with a resulting dc output voltage.

LC filter (or) L-Section filter :—

The ripple factor is directly proportional to the load resistance R_L in the inductor filter and inversely proportional to the R_L in the capacitor filter. If these two filters are combined then LC filter or L-section filter obtained. The ripple factor independent of R_L.

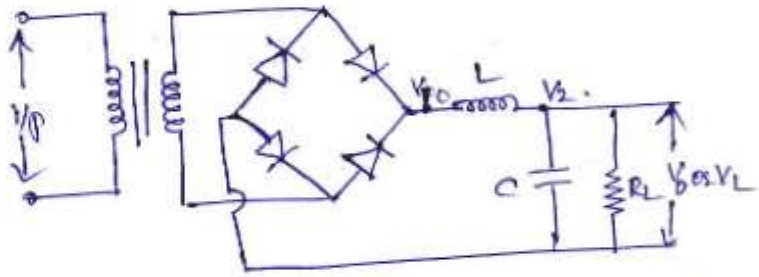


L-Section filter using full wave Rectifier

→ If the value of 'L' is increased it will increase the time of conduction. At some critical value of L one diode either D_1 or D_2 will always be in conducting.

· By applying fourier series analysis for the output of full wave rectifier we get

$$V_1 V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi} \sum_{k=even,(k\neq 0)} \frac{\cos k\omega t}{(k+1)(k-1)}$$



L-Section filter using Bridge Rectifier

$$V_{FO} V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t - \frac{4V_m}{15\pi}\cos 4\omega t - \frac{4V_m}{35\pi}\cos 6\omega t - \cdots$$

for higher order harmonic frequencies inductor offers high impedance so current cannot passes through the inductor for higher harmonic frequencies.

$$V_2 = \underbrace{\frac{2V_m}{\pi}}_{DC} - \underbrace{\frac{4V_m}{3\pi}\cos 2\omega t}_{AC}$$

V_2 is available at the prior to the capacitor i.e. prior to the capacitor there are two components one is dc component and the other is rms current.

capacitor blocks DC and allows AC signal i.e. rms current, the DC current passes through the load resistor. so the DC signal is appeared across the load.

$$\because V_{dc} = \frac{2V_m}{\pi}, \quad I_{rms} = \frac{4V_m}{3\pi\sqrt{2}} \cdot \frac{1}{X_L} \quad \text{since } I_{rms} = \frac{V_{rms}}{X_L}.$$

$$I_{rms} = \frac{2\sqrt{2}\,V_m}{3\pi X_L} = \frac{\sqrt{2}\,V_{dc}}{3X_L} \qquad \text{Since } V_{dc} = \frac{2V_m}{\pi}$$

This I_{rms} is available at prior to the capacitor. This current passes through the capacitor. then the voltage is developed across the capacitor. Ripple voltage developed across the capacitor due to

I_{rms} passes through the capacitor is

$$V_{r,rms} = I_{rms} \cdot X_C = \frac{\sqrt{2}\,V_{dc}}{3X_L} \cdot X_C = \frac{\sqrt{2}}{3} V_{dc} \frac{X_C}{X_L}$$

Since ripple factor $r = \frac{V_{r,rms}}{V_{dc}}$

$$\therefore \boxed{r = \frac{\sqrt{2}}{3}\frac{X_C}{X_L}}$$

if for case of
$X_L = \omega L$
$X_C = \frac{1}{\omega C}$

where $X_C = \frac{1}{2\omega C}$ & $X_L = 2\omega L$ for second harmonic frequencies.

$$r = \frac{\sqrt{2}}{3} \cdot \frac{1}{2\omega C * 2\omega L} = \frac{\sqrt{2}}{3}\frac{1}{4\omega^2 LC}$$

$$\boxed{r = \frac{\sqrt{2}}{3}\frac{1}{4\omega^2 LC}}$$

Bleeder Resistor:—

→ for a critical value of inductor either of the diodes is always conducting i.e., current does not fall to zero.

→ The incoming current consists of two components. They are

(i) $I_{dc} = \frac{V_{dc}}{R_L}$ (ii) A sinusoidal varying component with peak value of $\frac{4V_m}{3\pi X_L}$.

The negative peak of the current must always be less than dc i.e.

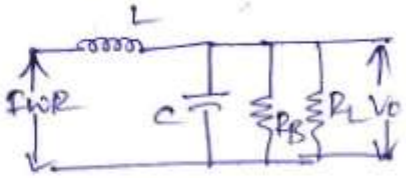
$\sqrt{2}\,I_{rms} \le \frac{V_{dc}}{R_L}$

for LC filter, $I_{rms} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L}$

Hence $\frac{2V_{dc}}{3X_L} \le \frac{V_{dc}}{R_L}$ i.e., $X_L \ge \frac{2}{3}R_L$

i.e., $\boxed{L_c = \frac{R_L}{3\omega}}$ where L_c is the critical inductance.

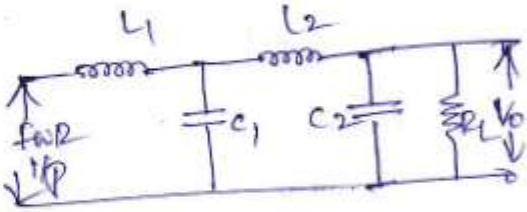
→ $X_L \geq \frac{2}{3} R_L$ cannot be satisfied for all load requirements. At no load i.e., $R_L = \infty$, the value of the inductance will also tend to be infinity. To overcome this a bleeder resistor R_B is connected in parallel with the load resistor. Therefore minimum current will always be present for optimum operation of the inductor. It improves voltage regulation of the supply by acting as the pre-load on the supply. It provides safety by acting as a discharging path for capacitor.



Multiple LC filters :—

Better filtering can be achieved by using two or more L-section filters. The ripple factor

$$r = \frac{\sqrt{2}}{3} \cdot \frac{X_{C2}}{X_{L2}} \cdot \frac{X_{C1}}{X_{L1}}$$



---

if $X_{C2} = X_{C1} = X_C$ & $X_{L2} = X_{L1} = X_L$ then

$$\boxed{r = \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L}\right)^2}$$

if there are n- number filters are connected in series then

$$\boxed{r = \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L}\right)^n}$$

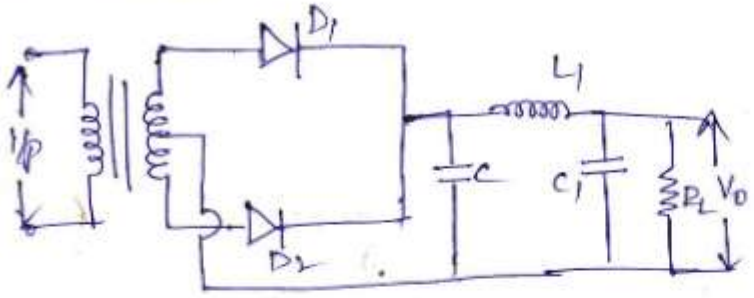
π - Section or CLC filter :—

→ In the LC filter or L-section filter there is some voltage drop across L. If this cannot be tolerated and more DC output voltage V_o is desired, CLC filter is to be used. The ripple factor will be the same as that of L-section but the regulation will be poor.

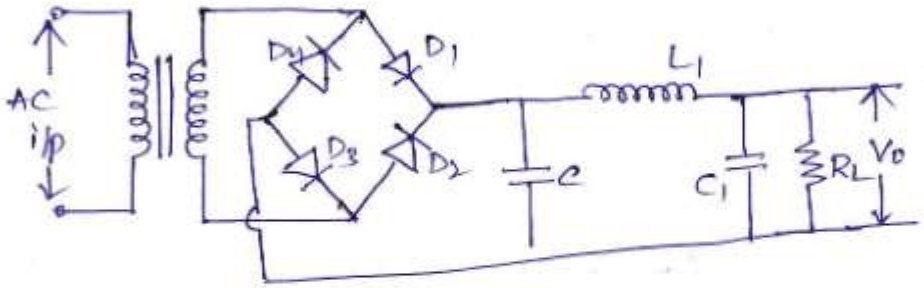
(13) In CLC, the output of the capacitor filter is the input for the L-section filter.

The output of capacitor filter is a triangular wave superimposed over DC.

Circuit Diagram :-



π - section filter using full wave Rectifier.

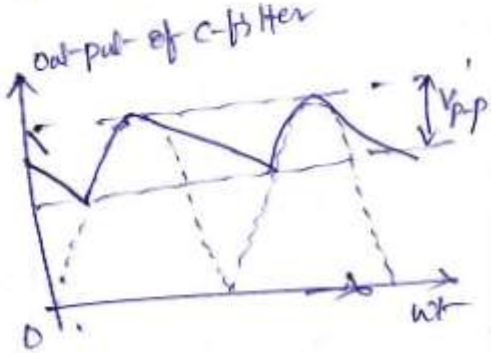


π- section filter using Bridge Rectifier.

→ The output of the capacitor filter is a triangular wave. This signal can be represented by fourier series as

$$V = V_{DC} - \frac{V'_{p-p}}{\pi}\left(\sin 2\omega t - \frac{\sin 4\omega t}{2} + \frac{\sin 6\omega t}{3} + \cdots\right)$$

where $V_{DC} = \frac{2V_m}{\pi}$, $V'_{p-p} = \frac{I_{dc}}{2fC}$



By a when this signal passes through the inductor, inductor offers high impedance for higher order harmonic components. So by neglecting higher order terms. The rms voltage of the second harmonic ripple is

$$\frac{V'_{p-p}}{\pi\sqrt{2}} = \frac{I_{DC}}{2\sqrt{2}\pi fC} = \frac{\sqrt{2}\,I_{DC}}{4\pi fC}$$

Since $X_C = \frac{1}{2\omega C} = \frac{1}{4\pi fC}$ for second harmonic

$\therefore V'_{rms} = \sqrt{2}\, I_{DC} X_C$

The output of capacitor filter is the input for the L-section filter of LC_1.

from L-section filter.

The current passes through the inductor $= \frac{\sqrt{2}\, I_{DC} X_C}{X_{L1}}$

The output voltage = Current * X_C

$$V'_{rms} = \frac{\sqrt{2}\, I_{DC} X_C}{X_{L1}} \cdot X_{C1}$$

$$\text{Ripple factor}(\gamma) = \frac{V'_{rms}}{V_{dc}} = \left(\frac{\sqrt{2}\, I_{DC} X_C}{V_{dc}}\right) \frac{X_{C1}}{X_{L1}}$$

$V_{dc} = I_{DC} \cdot R_L$

$$\therefore \boxed{\gamma = \frac{\sqrt{2} X_C}{R_L} \cdot \frac{X_{C1}}{X_{L1}}} \quad ***$$

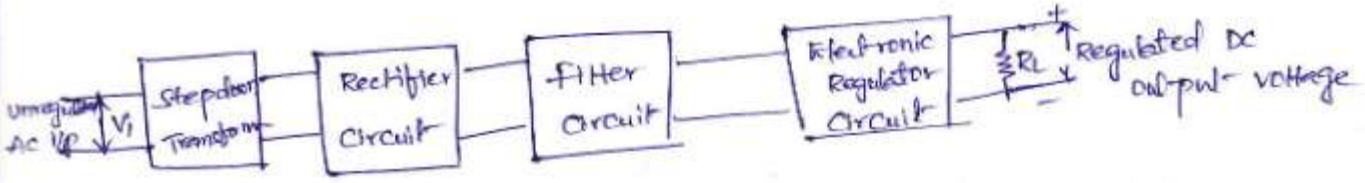
Where all reactances are calculated at the 2nd harmonic frequency $\omega = 2\pi f$.

Dc output voltage = (the DC voltage for a capacitor filter) − (the drop across L_1).

Voltage Regulation Using Zener Diode :—

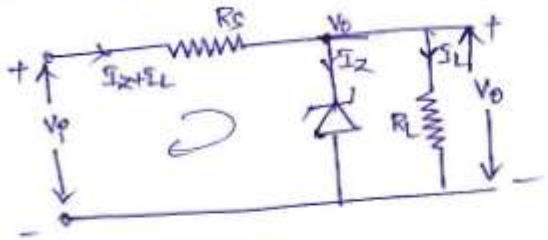
→ Voltage Regulator Circuits are electronic circuits which gives constant DC output voltage, irrespective of variations in input voltage V_i, current drawn by the load I_L from output terminals and Temparature T.

→ Voltage Regulator is used when the output delivered is DC voltage. The input can be DC which is not constant and fluctuating. If the input is AC, it is converted to DC by rectifier and filter circuits. and it is applied to the voltage Regulator circuit to get constant DC output voltage.



→ The voltage Regulator circuits are used for electronic systems, electronic circuits, IC circuits etc.

Circuit Diagram:-



By KVL,

$V_p - (I_Z+I_L) R_S - V_0 = 0$

$$V_0 = V_p - (I_Z+I_L) R_S$$

As the input voltage increases current passes through the Resistor R_S increases then the voltage developed across R_S increases. Then the voltage developed across the Load Resistor is constant.

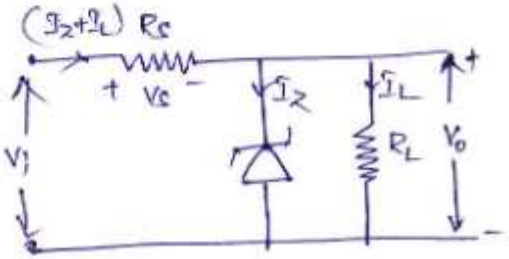
Let V_S is the current through the voltage developed across R_S when current passes through it i.e.,

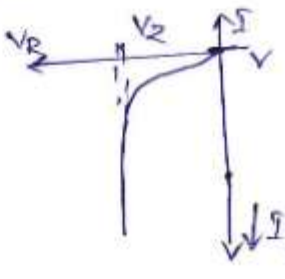
$$V_S = (I_Z+I_L) R_S$$

$\therefore V_0 = V_p - V_S$

Here as V_p increases, V_S also increases so V_0 is constant.

→ In the reverse characteristic voltage remains constant irrespective of the current that is flowing through zener diode. The voltage in the break down region remains constant.





The limitations of the circuit are:

→ the output voltage remains constant only when the input voltage is sufficiently large so that the voltage across the zener is V_z.

→ There is limit to the maximum current that we can pass through the zener. If V_i is increased, I_z increases and hence breakdown will occur.

→ Voltage regulation is maintained only between this limits, the minimum current and the maximum permissible current through the zener diode.

Introduction:-

A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name 'Bipolar'. The BJT is used in Amplifiers and oscillator circuits and as a switch in digital circuits. The BJT has wide applications in computers, satellites and other modern communication systems.

→ Transistor was invented by William Schokley, Bartain and Bardeen.

→ Transistor is a Current Controlled device (CCD).

The Junction Transistor:-

→ The three terminals of BJT are Emitter (E), Base (B) and Collector(C)

→ In these three terminal regions. Emitter is highly doped because to ingest (its majority (more) number of) carriers into the ~~Emitter~~ Base region and having medium Area.

→ Base is lightly doped to reduce the recombinations and is provided with smallest area to decrease the transit time. Transistor action takes place in the base region.

→ collector is moderately doped and psovided with largest area to overcome heat dissipation and to accomodate more number of charge carriers, since most of the charge carrier passes from the emitter into the collector.

→ In BJT, Emitter-Base junction is forward Biased and collector-Base junction is Reverse Biased. Due to the forward Bias on the emitter-Base junction, an emitter Current flows through the base into the collector. Through the collector-base junction is reverse biased, almost the entire emitter Current flows through the collector region.

→ Due to the Emitter - Base Junction is in forward Biased then the input side is having low resistance and collector - Base Junction is in Reverse bias so the output resistance is high. so for the transistor the input is having low resistance and the output is having high resistance. i.e. resistance of the transistor is transformed from low resistance to high resistance. so the device is called "Transistor".

Transfer + Resistor = Transistor.

→

J_E	J_C	operation of Transistor
forward Bias	forward Bias	Saturation Region
forward Bias	Reverse Bias	Active Region
Reverse Bias	Reverse Bias	Cut-off Region
Reverse Bias	forward Bias	Inactive Region

→ If both the Junctions are connected in forward bias then the transistor is operated in saturation region.

→ If both the Junctions are connected in Reverse Bias then the transistor is operated in Cutoff region.

→ If the Emitter - Base Junction (J_E) is connected in forward Bias and collector - Base Junction (J_C) is connected in Reverse Bias then the transistor is operated in Active Region. If the Junctions are connected in Reverse then the transistor is operated in Inactive region.

→ If Emitter - Base Junction (J_E) and collector - Base (Junction (J_C) are in forward Biased and if J_E voltage is greater then the collector Junction voltage. Then the transistor is operated in "forward saturation Region".

→ If Emitter - Base Junction (J_E) and collector - Base Junction (J_C) are in Reverse forward Biased and if J_E voltage is less then the J_C voltage then the transistor is operated in "Reverse saturation Region".

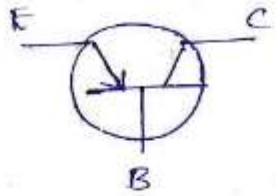
III (2)

→ There are two types of transistors. They are

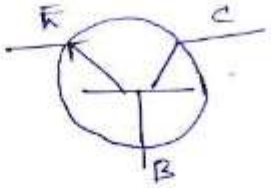
** NPN transistor

** PNP transistor.

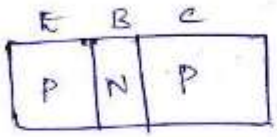
→ The symbol of the transistors are

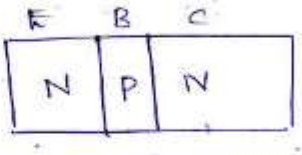


PNP transistor



NPN Transistor





If the arrow mark is towards the base it is PNP transistor and if the arrow mark is away from base then it is NPN transistor.

→ The arrow mark on the emitter specifies the direction of current when the emitter-base junction is forward Biased.

When the PNP transistor input side is in forward Biased, then the holes are injected into the base. So the holes move from emitter to base. The conventional current flows in the same direction as holes. So arrow mark towards the base for PNP transistor. Similarly for NPN transistor it is away from the Base.

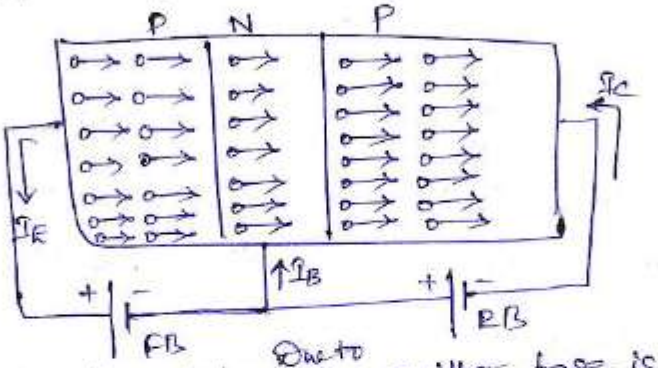
→ When two diodes are connected in back to Back the diode equivalent circuit cannot function as a transistor, because

(i) there is no bonding force in between the two diodes

(ii) the base width will become very large so that no charge carriers will be reaching the collector.

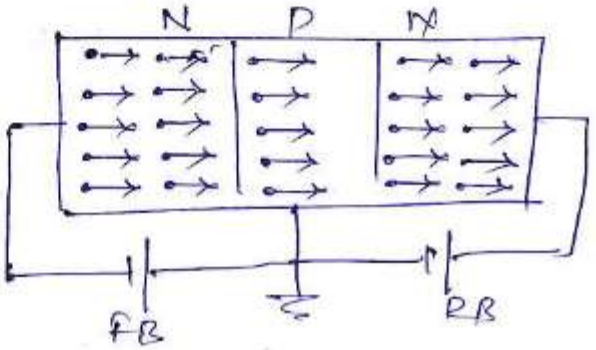
→

→ for a PNP transistor, the emitter-Base is forward Biased, collector Base junction is Reverse Biased. Due to the forward Biased applied to the emitter-Base junction of PNP transistor causes a lot of holes from the emitter region to crossover to the base region. As the base is lightly doped with n-type impurity, the number of electrons in the base region is very small and hence the number of holes that combine with electrons in the n-type base region is also very small. Hence a few holes combines with electrons to constitute a base current I_B. The remaining holes cross over into the collector region to constitute a collector current (I_C). Thus the base and collector current summed up gives the emitter current i.e. $I_E = -(I_B + I_C)$.

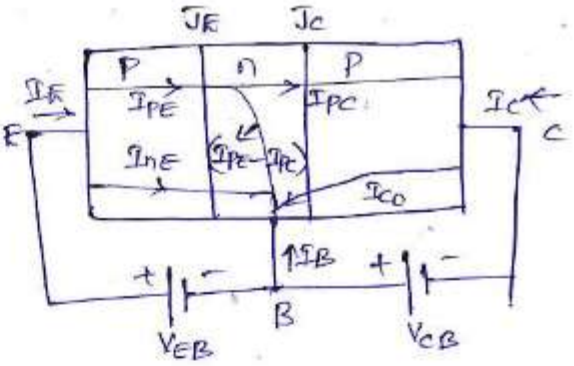


→ for a NPN transistor, the emitter base is forward biased. Due to lot of electrons from the emitter region to cross over to the base region. As the base is lightly doped with p-type impurity, the no. of holes in the base region is very small and hence the number of electrons that combine with holes in the p region p-type base region is also very small. Hence a few electrons combine with holes to constitute a base current I_B. The remaining electrons cross over into the collector region to constitute a collector current I_C. Thus the base and collector current summed up gives the emitter current i.e.,

$I_E = -(I_C + I_B)$.



Transistor Current Components :—



Here the input is connected in forward Bias and output is connected in Reverse Bias. The Emitter Current I_E consists of hole Current I_{PE} (holes crossing from emitter into Base) and electron Current I_{nE} (electrons crossing from base into the Emitter). The ratio of I_{PE}/I_{PE} crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n-material.

In pnp transistor, the emitter Current consists almost entirely of holes. i.e. most of the holes from Emitter region are crossing the junction and enters into the Base region. Not all the holes crossing the emitter junction J_E reach the collector junction J_C because some of them combine with the electrons in the n-type base. If I_{PC} is the hole Current at J_C, there must be bulk recombination Current $(I_{PE} - I_{PC})$ leaving the base.

If the Emitter were open circuited so that $I_E = 0$ then I_{PC} would be zero. Under these circumstances, the base and collector would acts as reverse biased diode, and the collector Current I_C would equal the reverse saturation Current I_{CO}.

If $I_E = 0$, $I_C = I_{CO}$.

if $I_E \neq 0$, $I_C = I_{CO} - I_{PC}$.

for a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right and electrons crossing J_C in the opposite direction.
for a pnp transistor, I_{CO} is negative and for npn transistor, I_{CO} is positive.

Emitter Efficiency :— (or) Injection Efficiency (γ)

$$\gamma = \frac{\text{Current due to injected carriers at } J_E}{\text{Total emitter Current}}$$

In the case of pnp transistor we have

$$\boxed{\gamma = \frac{I_{PE}}{I_{PE} + I_{nE}} = \frac{I_{PE}}{I_E}}$$

I_{PE} → Injected hole diffusion Current at Emitter Junction
I_{nE} → Injected electron diffusion Current at Emitter Junction.

Transportation factor (β^*):

$$\beta^* = \frac{\text{Injected carrier current reaching } I_C}{\text{Injected carrier current at } I_E}$$

In the case of pnp transistor we have

$$\boxed{\beta^* = \frac{I_{pC}}{I_{pE}}}$$

Large signal current Gain:

It is the ratio of the negative of the collector current increment to the emitter current change from zero (cut off) to I_E as the large signal current gain of a common base transistor i.e.

$$\alpha = -\frac{I_C - I_{CO}}{I_E}$$

Since I_C & I_E have opposite signs. then α is always positive.

$\alpha \rightarrow 0.90$ to 0.995.

$$\therefore \alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{pE}} \cdot \frac{I_{pE}}{I_E}$$

$$\boxed{\alpha = \beta^* \gamma}$$

Transistor As an Amplifier:

A small change ΔV_i of Emitter Base voltage causes relatively large Emitter current change ΔI_E. α' is defined as the ratio of the change in collector current to the change in Emitter current. Because of change in Emitter current ΔI_E and consequent change in collector current. There will be change in output voltage ΔV_o.

Since $\alpha' = \frac{\Delta I_C}{\Delta I_E}$

$\Delta V_o = \alpha' \cdot R_L * \Delta I_E$

$\Delta V_i = r_e' \cdot \Delta I_E$

where
$\alpha' \rightarrow$ small signal forward circuit current Gain
$r_e' \rightarrow$ Emitter Junction resistance
$R_L \rightarrow$ Load resistance.

Voltage Amplification is,

$$A_V = \frac{\Delta V_o}{\Delta V_i} = \frac{\alpha' R_L \cdot \Delta I_E}{r_e' \cdot \Delta I_E} = \frac{\alpha' R_L}{r_e'}$$

$$\boxed{A_V = \frac{\alpha' R_L}{r_e'}}$$

Since the input is connected in forward Bias so the input resistance is very less.

Where $R_L \gg r_e'$,

$$\therefore \boxed{A_V > 1} \Rightarrow \boxed{V_o > V_i}$$

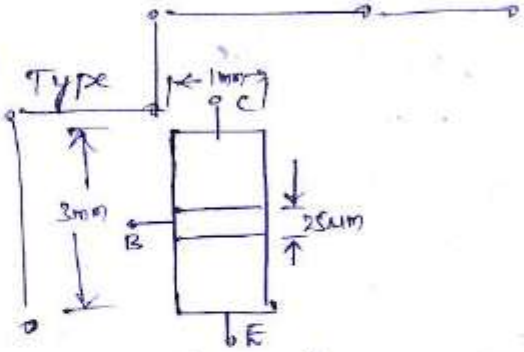
So a small change in V_{BE} produces the large change in V_{CB}. Hence the transistor acts as an amplifier.

Transistor construction :-

→ Transistor is made up of semiconductor materials i.e. Si or Ge. These transistors can be constructed by different methods.

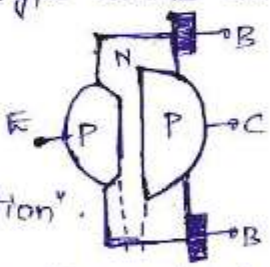
They are

- → Grown type
- → Alloy type
- → Electrochemically Etched Type
- → Diffusion Type
- → Epitaxial Type.



→ (i) Grown Type:-

The NPN grown junction transistor is made by drawing a single crystal from a melt of silicon or Ge whose impurity concentration is changed during the crystal drawing operation by adding n or p-type atoms as required.



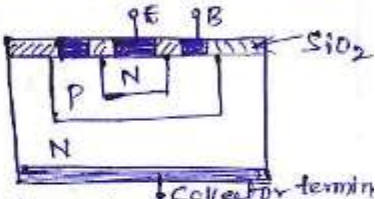
(ii) Alloy Type:- This technique also called "fused construction". For a PNP transistor, the center (base) section is a thin wafer of n-type material. Two small dots of indium are attached to the opposite sides of the wafer and the whole structure raised for a short time to a high temperature above the melting point of Indium but below that of Ge. The Indium dissolves the Ge beneath it and forms a saturation solution. On cooling, the Ge in contact with the base material recrystalizes with enough Indium concentration to change it from n-type to p-type. The collector is made larger than the Emitter, so that emitter collector subtends a large angle viewed from Emitter. So very little emitter current follows a diffusion path which carries it to base.

(iii) Electrochemically Etched type:—

This technique consists of etching depressions on opposite sides of a semiconductor wafer in order to reduce the thickness of this base section. The emitter and collector junctions are then formed by electroplating a suitable metal into the depression Areas. This type of devices referred to as a Surface barrier transistor.

(iv) Diffusion Type:—

In this process the base collector junction area is determined by a diffusion mask which is photo etched just prior to the base diffusion. The emitter is then diffused on the base and final layer of SiO_2 is thermally grown over the entire surface. Because of the passivating action of this oxide layer, most surface problems are avoided and very low leakage currents result. There is also an improvement in the current gain at low currents and in the noise figure.



(v) Epitaxial Type:— (Epi = ON, Taxi ⇉ Arrangement)

The epitaxial technique consists in growing a very thin, high purity single crystal layer of Si or Ge on a heavily doped substrate of the same material. This augmented crystal forms the collector on which the base and emitter may be diffused.

Types of configuration:—

When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output. Depending upon the input and output and common terminal a transistor can be connected in three configurations. They are

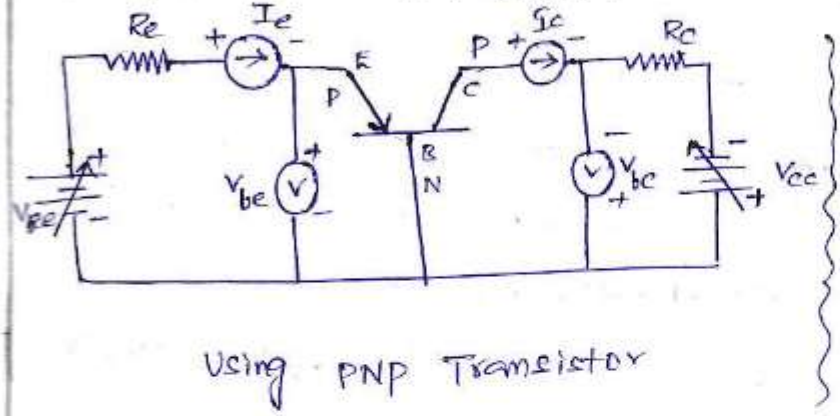
(i) Common Base (CB) Configuration

(ii) Common Emitter (CE) Configuration

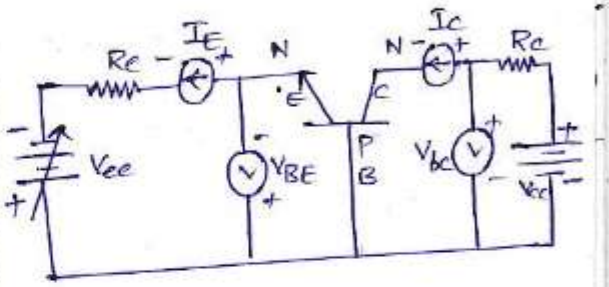
(iii) Common Collector (CC) Configuration.

→ In any transistor configuration, many different families of characteristic curves can be drawn, depending upon which two parameters are chosen as the independent variables. Generally the input current and output voltage are the independent variables. The output current and the input voltage are expressed graphically in terms of these independent variables. So the output current and the input voltage are depends on independent variables so these are the Dependent variables.

Common Base Configuration :-



Using PNP Transistor

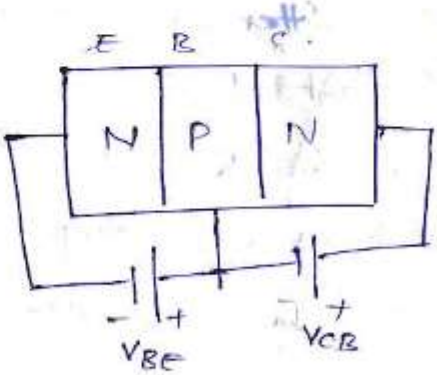


Using NPN transistor.

→ This is also called grounded Base configuration. In this configuration, Emitter is the input terminal, collector is the output terminal and base is the common terminal.

→ Input is connected in forward Bias and output side is connected in Reverse Bias.

→ If we consider the NPN transistor.



Input characteristics :-

To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volt and observe the values of V_{BE} and I_E by changing the supply voltage. $V_{CB} = 0$ means that output is shorted i.e. no biasing is applied to the output. Then this transistor acts as a PN function diode with forward biasing. So the characteristics of

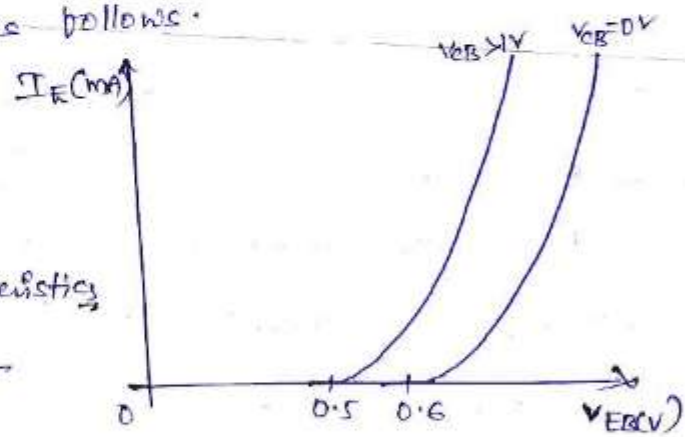
Transistor are same as the characteristics of diode i.e, Current increases exponentially with the input voltage.

As the output voltage (V_{CB}) increases, the depletion layer width between base and collector increases because of reverse bias. then the collector region penetrates into the base. so the base region reduces. Then the recombinations reduces. In NPN transistor, Electrons flows from input side to the output side [i.e, Emitter to Collector] so the direction of Current from collector to Emitter.

As the reverse bias voltage increases more number of carriers are injected into the Emitter are diffused into the base are attracted by the supply. so Current increases across ~~collector and~~ Emitter Junction i.e, I_E increases.

Therefore the emitter Current increases with $V_{BC}^{(V)}$ and $V_{BE}^{(V)}$.

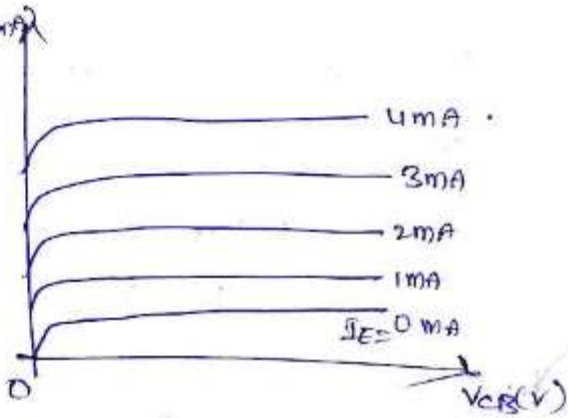
The Input characteristics are as follows:



Output characteristics: —

To determine the output characteristics the emitter Current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitably equal steps and the collector Current I_C is observed for each value of I_E. This is repeated for different fixed values of I_E.

When Input Current $I_E = 0$ i.e, $V_{BE} = 0$. i.e, the transistor input is shorted so the transistor acts as a PN diode with reverse bias connected. So the Current passes through the collector Junction is due to minority carriers so the Current is reverse saturation Current.



When $I_E = 0$ i.e., the input Current is zero through the Emitter-Base Junction is zero then the Current through the collector-Base junction is due to the minority carriers because of reverse bias connection. So small amount of Current passes through the Base-Collector Junction. As Reverse Bias Voltage increases then the depletion layer width between Base and Collector increases. Since Base is lightly doped than the collection region. So most of the depletion layer penetrates into the Base region, therefore width of the base region reduces then the base Current in the base region reduces. which is in the order of micro Amperes (μA). This minority carrier Current along Base-collector junction is not much affected by the reverse Bias voltage but much affected by the temperature. Irrespective of reverse Bias voltage, the Current is constant.

→ When I_E increases i.e., input Current increases and as the reverse bias voltage increases Base Current (I_B) reduces. Then the collector Current ($i_C = i_E - i_B$) constant since I_B independent of voltage, i_B is constant. I_C value depends on Emitter Current.

Early Effect (or) Base Width Modulation. ——

As the collector voltage V_{CE} is made to increase the reverse bias, the space charge width between collector and base tends to increase with the result that the effective width of the base decreases. This dependancy of Base width on collector to Emitter voltage is known as the "Early Effect".

→ The decrease in effective base width has three consequences:

(i) There is less chance for recombination with the base region. Hence 'α' increases with increasing V_{CB}.

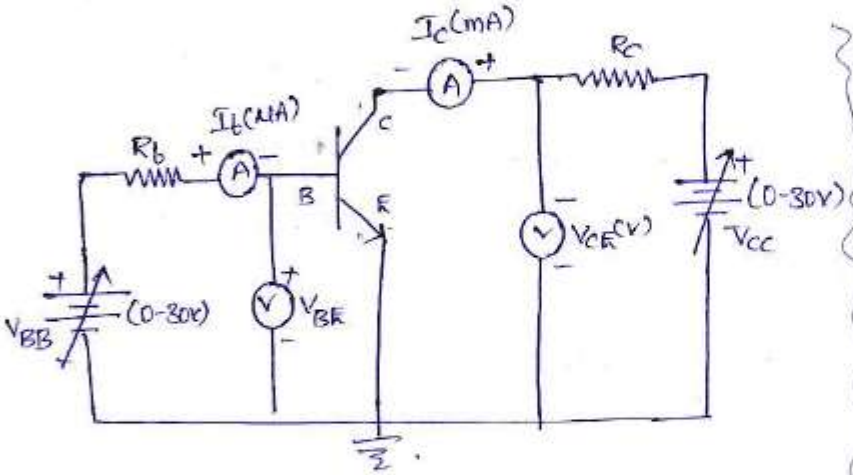
(ii) The charge gradient is increased within the base and consequently the Current of minority carriers injected across the emitter Junction increases.

(iii) for extremely large voltages, the effective base width may be reduced to zero, causes voltage breakdown in the transistor. This phenomena is called the "punch through".

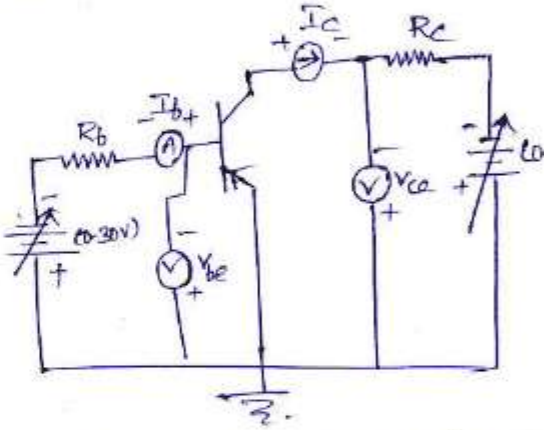
for higher values of V_{CB}, due to Early Effect, the value of 'α' increases. for example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

Common Emitter Configuration:

This is also called as 'Grounded Emitter configuration'. In this configuration base is the input terminal, collector is the output terminal and emitter is the common terminal.



CE transistor using npn transistor



CE transistor using pnp transis

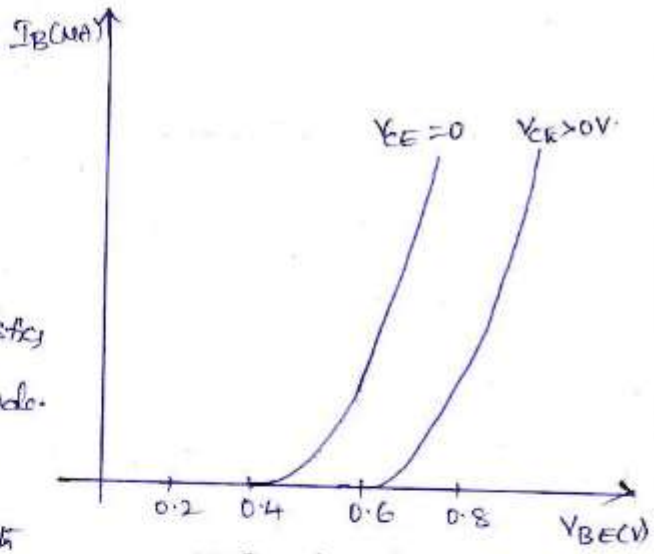
→ In CE, Dependent parameters are input voltage (V_{BE}) and output current (I_C). Independent parameters are input current (I_B) and output voltage (V_{ce}).

Input characteristics:

To determine the input characteristics, keep the output voltage (V_{ce}) as constant and by changing the supply voltage V_{BB} from 0 to 30V, observe the values of V_{BE} (V) and I_b (μA) [i.e, input voltage (V_{BE}) and Input Current (I_B)]. Similarly observe the values of V_{BE} and I_b for different higher fixed values of V_{ce}. As the input supply increases then I_B increases with the input voltage V_{BE}. when input voltage is less than the cut in voltage of the diode, the conduction is zero.

CE
Unit 7

When the applying supply input increases, V_{BE} increases then corresponding i_b also increases.

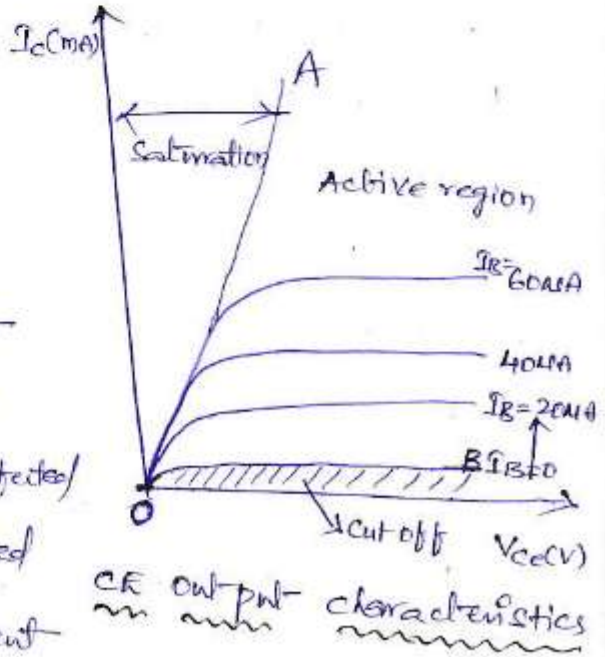


CE input characteristics

At $V_{CE}=0$ i.e., the output is open terminal and input is connected in forward Bias then the transistor characteristics similar to the characteristics of forward Biased PN Junction Diode. As we increase V_{CE} above 0 volts [i.e reverse voltage increases] the width of the base reduces with increase in Reverse Bias output voltage. As the width of the base reduces then the base current decreases with increase in Reverse Bias voltage.

Output characteristics :—

To determine the output characteristics, keep the input current & constant and By changing the supply voltage connected to the output circuit, observe the values of V_{ce}(V) and I_c(mA) [i.e out voltage (V_{ce}) and output current (I_c)]. Repeat same for different values of input current I_b(MA).



CE output characteristics

When I_B is constant, if we increases V_{ce} (i.e, output voltage) then the current doesnot affected because at Base_Collector Junction resultant current is a combination of minority carrier current. This current is not affected by the voltage. only (depends on) affected by the temperature. so collector current is constant when i_B is constant.

If we keep input current i.e. I_B constant at higher value then as V_{CE} increases I_C increases.

Common Collector Configuration:

→ The output characteristics of CE transistor configuration have three regions, namely, saturation region, cut-off region and active region.

The region of curves to the left of the line OA is called the 'saturation Region' and the line OA is called the 'saturation line'. In this region, both junctions are forward Biased and an increase in the base current does not cause a corresponding large change in I_C. The ratio of $V_{CE}(sat)$ to I_C in this region is called 'saturation Resistance'.

→ The region below the curve for $I_B=0$ is called the "cut off region". In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is off. Hence the collector current becomes almost zero and the collector voltage almost equals V_{CC}, the collector supply voltage. The transistor is virtually an open circuit between collector and emitter.

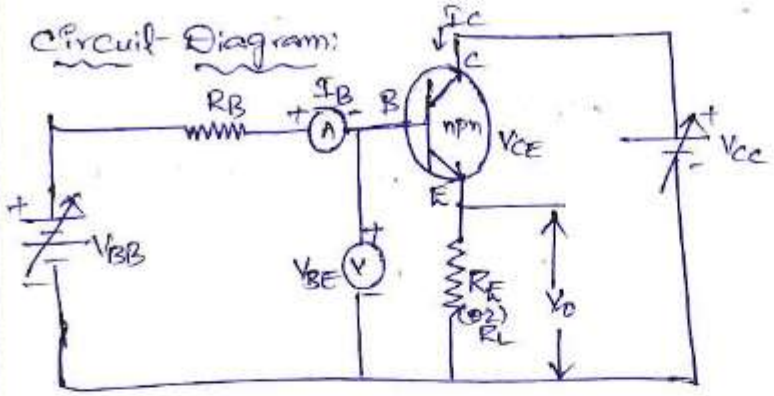
→ The central region where the curves are uniform in spacing and slope is called the 'Active region'. In this region, emitter-base junction is forward biased and the collector-Base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the Active region.

→ If the base current is subsequently driven large and positive, the transistor switches into the saturation region via the active region, which is traversed at a rate that is dependent on factors such as gain and frequency response.

Common collector Configuration :—

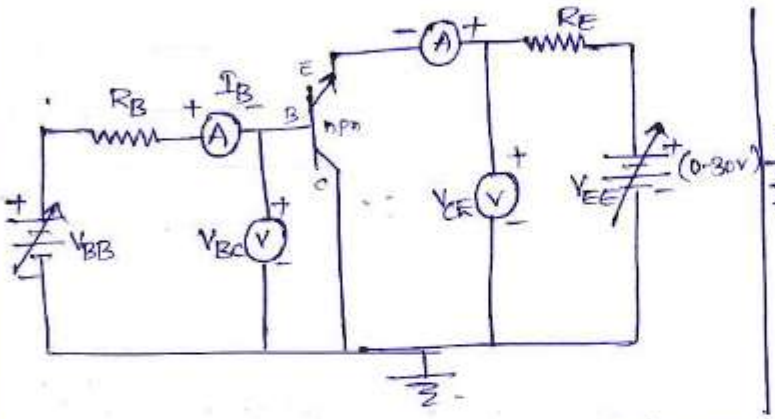
This is also called 'Grounded collector configuration'. In this configuration base is the input terminal, Emitter is the output terminal and collector is the common terminal.

Circuit Diagram:

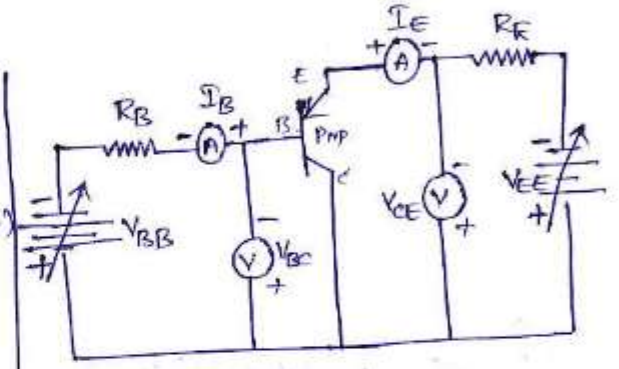


→ Dependent parameters:
V_{BE} & I_C

→ Independent parameters:
I_B, V_{CE}.



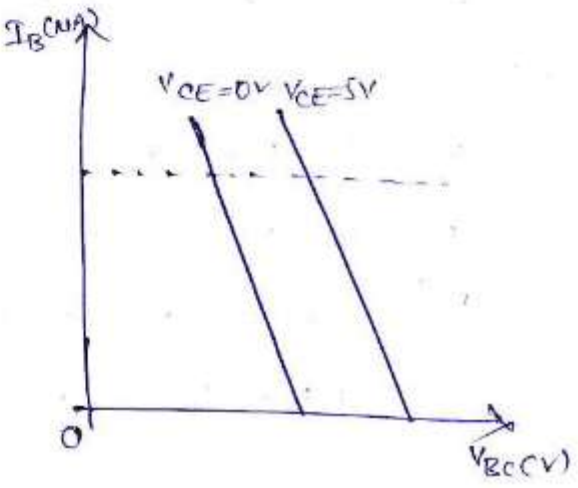
CC Circuit Diagram Using NPN Transistor



CC circuit Diagram using PNP transistor

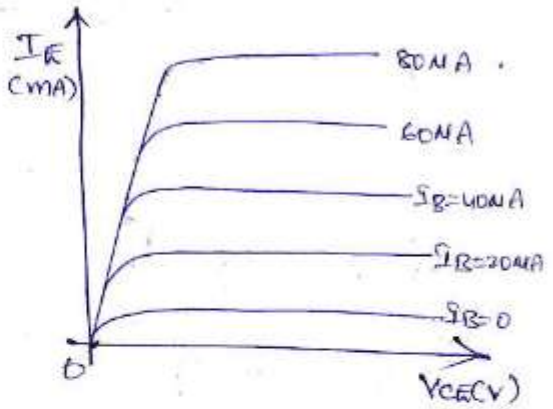
Input characteristics :—

To determine the input characteristics, V_{CE} is kept at suitable fixed value. By increasing the Base collector voltage V_{BC} in equal increamental steps and observe the corresponding I_B value. This is repeated for different fixed values of V_{CE}. Plots of V_{BC} versus I_B for different values of V_{CE} shown in figure.



Output characteristics:—

To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting the base collector voltage. Then the By increasing the collector-Emitter voltage (V_{CE}) in equal increamental steps observe the corresponding I_E values. Now the curves of I_E versus V_{CE} are plotted for different constant values of I_B.



Limits of operation:—

→ BJT can be used as an amplifier in the active region only. In this region for a small increase in input base current I_B large increase in output current I_C results. Thus giving amplification.

→ BJT can be used as a switch by operating between Cut-off and saturation regions. When the BJT is in saturation region, it can be considered to be 'ON' and when it is in Cut-off region it is considered to be 'OFF'.

→ Because of the Junction capacitances, a normal BJT can be used in Audio frequency (AF) range only. High frequency or RF transistors are designed and fabricated specially to have low capacitances values to enable usage in high frequency range. The hybrid model of BJT is valid in the AF range.

Specifications of BJT:-

S.No.	parameter	Symbol	Typical Value	units
1	Collector-Emitter Voltage	V_{CE}	40	V
2	Collector - Base Voltage	V_{CB}	60	V
3	Emitter - Base Voltage	V_{EB}	6	V
4	Collector Current	I_C	500	mA
5	Total power Dissipation	P_D	0.4	W
6	operating Temperature	T_{op}	25-80	°C
7	collector-Emitter Breakdown Voltage	BV_{CEO}	40	V
8	Emitter - Base Breakdown Voltage	BV_{EBO}	50	V
9	Current-Gain Bandwidth product	f_T	250	MHz
10	Output Capacitance	C_o	8	Pf
11	Input Capacitance	C_{in}	20	Pf
12	Small Signal Current-Gain	h_{fe}	100	-
13	Out-put admittance	h_{oe}	10	mU
14	Voltage feedback ratio	h_{re}	8×10^{-4}	-
15	Input Impedance	h_{ie}	3	kΩ
16	Delay Time	t_d	10	nsec.
17	Rise Time	t_r	20	nsec.
18	fall Time	t_f	50	nsec.
19	storage time	t_s	200	nsec
20	Noise figure	NF	4	dB.

BJT Hybrid Models:-

→ Small signal operation is that in which AC input signal voltages and currents are very small i.e., in the order of ±10% of Q-point voltages and currents.

→ The Equivalent circuit will aid in analysing transistor circuits easily and rapidly.

→ A transistor can be treated as two-port network. The terminal behavior of any two port network can be specified by the terminal voltages V_1 and V_2 at ports 1 and ports 2 respectively and currents i_1 and i_2 entering ports 1 and 2 respectively. Of these four variable V_1, V_2, i_1 and i_2 two can be selected as independent variables and remaining two can be expressed interms of these independent variables. This leads to various two port parameters out of which the following three are more important:

(1) z-parameters (or) Impedance parameters
(2) y-parameters (or) Admittance parameters
(3) H-parameters (or) Hybrid parameters.

Hybrid parameters:→

General equations when the input current 'i_1' and the output voltage 'V_2' are taken as independent variables and the input voltage 'V_1' and output current 'i_2' can be written as

$$V_1 = h_{11} i_1 + h_{12} V_2$$
$$i_2 = h_{21} i_1 + h_{22} V_2$$

$h_{11} = \left.\frac{V_1}{i_1}\right|_{V_2=0}$ → input impedance with output short

$h_{22} = \left.\frac{i_2}{V_2}\right|_{i_1=0}$ → output admittance with input open

$h_{12} = \left.\frac{V_1}{V_2}\right|_{i_1=0}$ → Reverse voltage transfer ratio with input open.

$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2=0}$ → forward current gain with output short.

→ i = I = input, o = 22 = output, f = 21 = forward transfer, r = 12 = Reverse transfer

→ for the transistor characteristics, input current and output voltage are the independent variables, input voltage and output current are the dependent variables same as hybrid parameters. So Transistors are designed

as hybrid parameters for easy of analysis.

→ for the transistor hybrid model.

h_i → short circuit input impedance, h_o → open circuit out-put admittance

h_r → open circuit reverse voltage transfer ratio = h_{12}

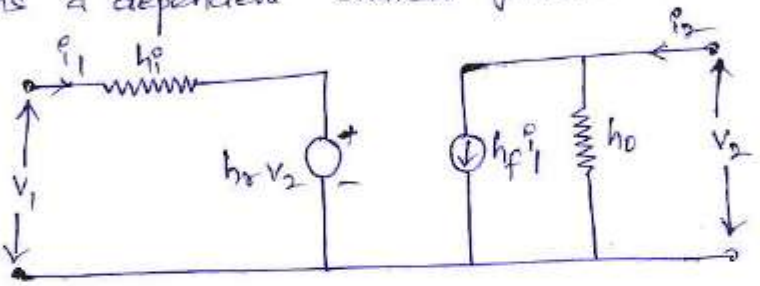
h_f → h_{21} = short circuit forward current gain.

$\therefore V_1 = h_i i_1 + h_r V_2$

$i_2 = h_f i_1 + h_o V_2$

These two equations can be verified by KVL in the input loop and KCL in the out-put node.

→ input circuit have a dependent voltage generator and the out-put circuit contains a dependent current generator.



Advantages of h-parameters:-

→ h-parameters are real numbers upto radio frequencies.

→ they are easy to measure.

→ they can be determined from the transistor static characteristics curves.

→ they are convenient to use in the circuit analysis and design.

→ Easily convertable from one configuration to other.

→ They are readily supplied by manufacturers.

Transistor in Common Emitter Configuration :—

The variables are i_b, i_c, V_{be} and V_{ce}. we can select i_b and V_{ce} as independent parameters.

$\therefore V_{be} = f_1(i_b, V_{ce})$ ——— (1)

V_{be} depends on i_b and voltage across collector and emitter is V_{ce},

$$i_c = f_2(i_b, V_{ce}) \longrightarrow (2)$$

Making a Taylor series expansion of (1) & (2), and neglecting higher order terms.

$$\Delta V_{be} = \frac{\partial f_1}{\partial i_B}\bigg|_{V_{ce}} \Delta i_b + \frac{\partial f_1}{\partial V_{ce}}\bigg|_{I_b} \Delta V_{ce}$$

$$\Delta i_c = \frac{\partial f_2}{\partial i_B}\bigg|_{V_{ce}} \Delta i_b + \frac{\partial f_2}{\partial V_c}\bigg|_{i_b} \Delta V_{ce}$$

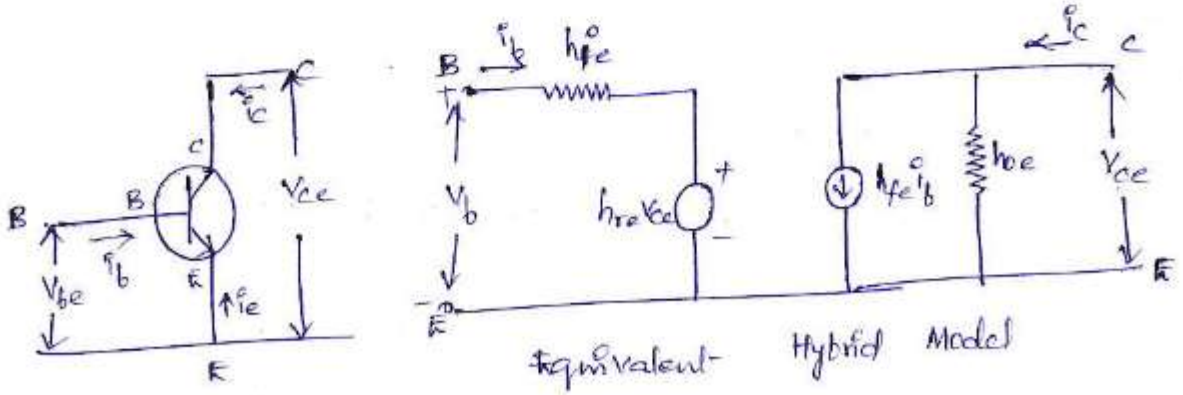
$\Delta V_{ce}, \Delta i_c$ are AC quantities [incremental variations in DC quantities]. The quantities ΔV_{be}, Δi_b, ΔV_{ce} and Δi_c represent small signal base and collector voltages and currents. They are represented as V_{be}, i_b, V_{ce} and i_c.

$$\therefore V_{be} = h_{ie} i_b + h_{re} V_{ce}$$

$$i_c = h_{fe} i_b + h_{oe} V_{ce}$$

where $h_{ie} = \frac{\partial f_1}{\partial i_b} = \frac{\partial V_b}{\partial i_B}\bigg|_{V_{ce}=K}$, $h_{re} = \frac{\partial V_B}{\partial V_c}\bigg|_{I_B=K}$

$$h_{fe} = \frac{\partial i_c}{\partial i_B}\bigg|_{V_{ce}=K}, \quad h_{oe} = \frac{\partial i_c}{\partial V_c}\bigg|_{i_b=K}.$$

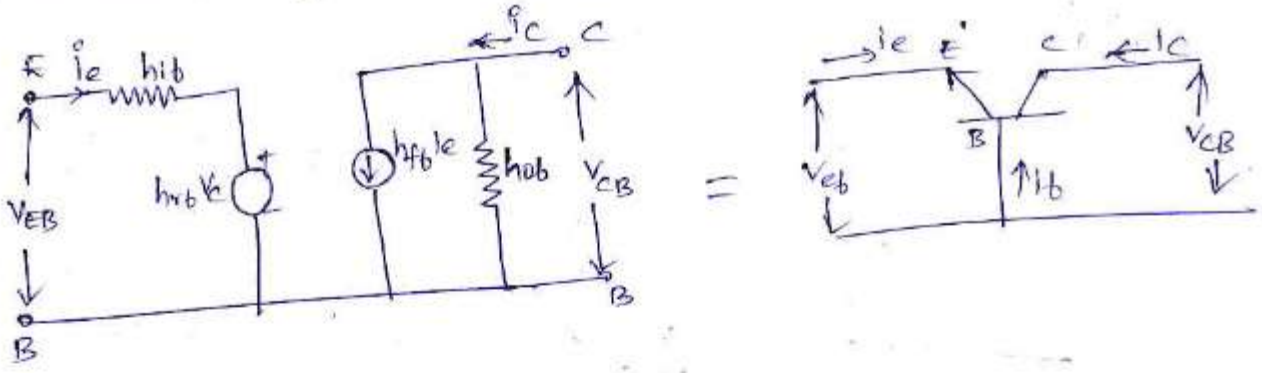


Equivalent Hybrid Model

By KVL at the input — $V_{be} = h_{ie} i_b + h_{re} V_{ce}$

By KCL at the output node — $i_c = h_{fe} i_b + h_{oe} V_{ce}$.

(ii) Common Base configuration:—

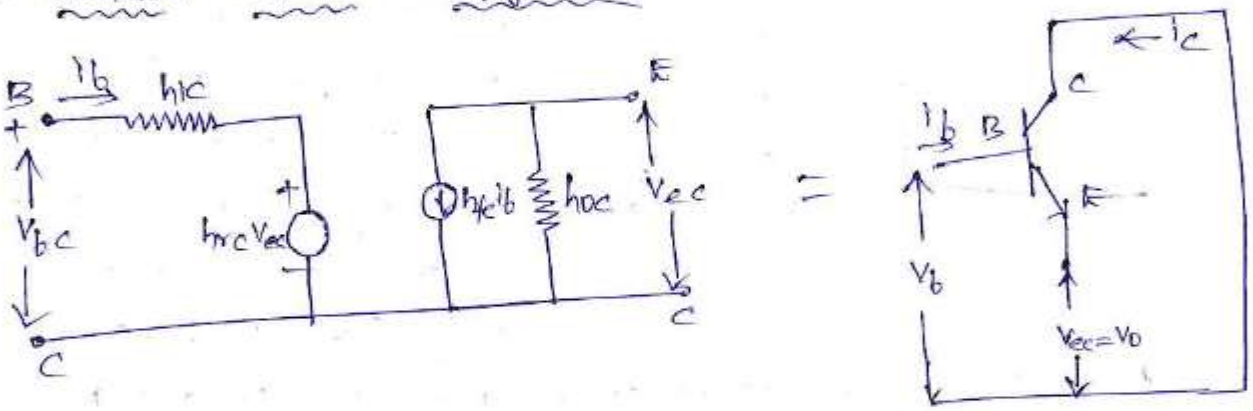


The equations are $V_{eb} = h_{ib} i_e + h_{rb} V_{CB}$

$i_c = h_{fb} i_e + h_{ob} V_{CB}$.

The above circuit is valid for NPN or PNP transistors. for PNP transistor, the direction of current will be different from NPN transistor.

(iii) common collector configuration:—



Equations are,

$V_{bc} = h_{ic} I_b + h_{rc} V_{ec}$

$I_e = h_{fc} I_b + h_{oc} V_{ec}$.

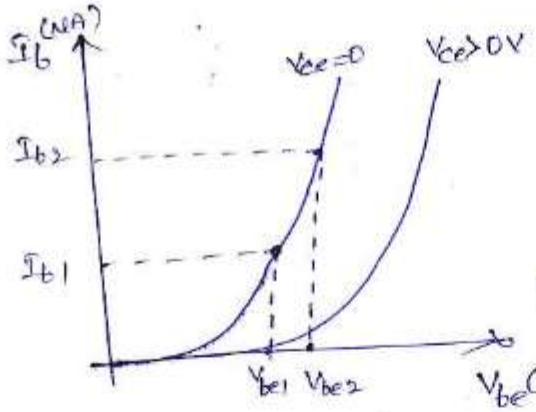
Determination of h-parameters from transistor characteristics:—

From input & the output characteristics of transistor, we can calculate hybrid parameters.

If we consider CE transistor,

- from the input characteristics we can calculate hie [input impedance) and hre (reverse voltage gain).
- from the output characteristics we can calculate hfe [forward current gain) and hoe [output admittance].

If we take
Input characteristics

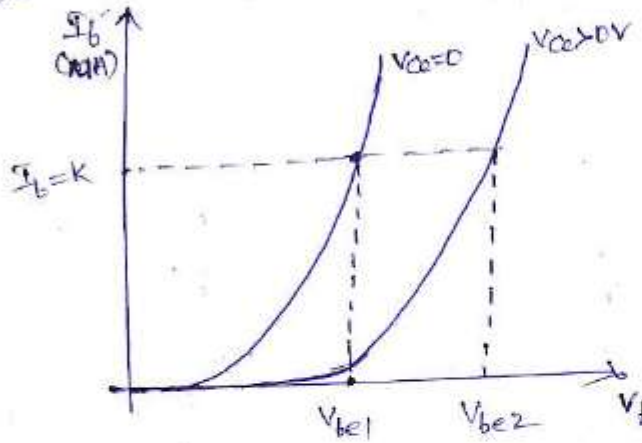


If we consider $V_{ce}=0$ Curve. observe the I_b values for different values of V_{be} respectively. The ratio of variation in V_{be} to variation in I_b (by keeping V_{ce} as constant) gives the input impedance hie.

$$\therefore h_{ie} = \frac{\Delta V_{be}}{\Delta I_b} = \frac{V_{b2}-V_{b1}}{I_{b2}-I_{b1}}$$

→ Similarly we can also calculate for any constant V_{ce} Curve.

→



→ If we consider any [reference] constant Current I_b(μA). If we project a line from that current along V_{be}, many ↑ Curves (constant V_{ce}) can intersect that constant Current line. Take any two intersecting points of constant Current and constant Voltage [V_{ce}] Curves. project lines from those intersecting points onto the V_{be} axis. which can occur at two different points on V_{be}(V). To calculate h_{re} (reverse voltage gain) take the ratio of variation in our input voltage (V_{be}) to variation in output voltage [V_{ce}] at I_b=constant. Since

$$h_{re} = \left.\frac{\Delta V_{be}}{\Delta V_{ce}}\right|_{I_B=\text{constant}(K)} = \frac{V_{be2}-V_{be1}}{V_{ce2}-V_{ce1}}$$

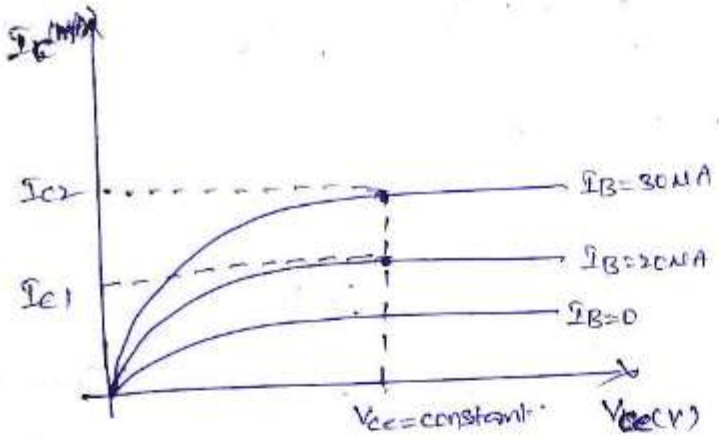
You can Calculate h_{re} for any value of I_b.

If we take output Characteristics

If we observe output characteristics of CE transistor. At particular constant value of V_{ce} project a line ↑ along I_c onto the different curves of I_b. Take any two constant value curves of I_b. project a lines on to the I_c from the intersecting points of constant I_b and V_{ce}.

DC
U-III-(12)

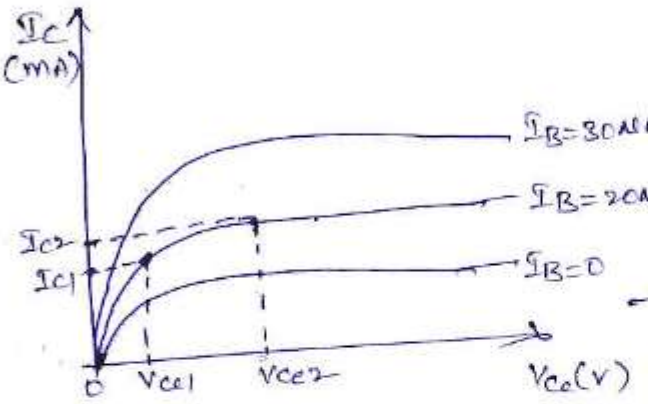
→



the ratio of variation in output current to the variation in input current by keeping V_{ce} constant gives the forward current Gain 'h_{fe}'.

Since $h_{fe} = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{ce}=K} = \left.\frac{i_{c2}-i_{c1}}{i_{b2}-i_{b1}}\right|_{V_{ce}=K}$.

→



→ Let us take input current i.e, I_b constant curve for various values of V_{ce} will get various current values I_c.

→ Ratio of the variation in output current (I_C) to the variation in output voltage by keeping I_B constant gives the output admittance.

Since $h_{oe} = \left.\frac{\Delta I_c}{\Delta V_{ce}}\right|_{I_B=K} = \left.\frac{I_{c2}-I_{c1}}{V_{ce2}-V_{ce1}}\right|_{I_B=K}$.

In this way, we can calculate hybrid parameters for any transistor configuration.

Conversion formulae for Hybrid parameters:—

CE to CC	CE to CB
$h_{ic} = h_{ie}$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
$h_{rc} = 1$	$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$
$h_{fc} = -(1+h_{fe})$	$h_{fb} = -h_{fe}/(1+h_{fe})$
$h_{oc} = h_{oe}$	$h_{ob} = h_{oe}/(1+h_{fe})$

Comparison of CB, CE and CC amplifier Configurations:-

CB Amplifier	CE Amplifier	CC Amplifier
→ Lowest input impedance	→ Moderate input resistance	→ Highest input resistance
→ Highest output resistance	→ Moderate output resistance	→ Lowest output resistance
→ Lowest Current Gain	→ Moderate current gain	→ Highest Current Gain
→ Highest Voltage Gain	→ Moderate voltage gain	→ Lowest voltage gain
→ phase shift is 0°	→ Highest power gain	→ Lowest power gain.
→ Moderate power gain.	→ phase shift is 180°	→ phase shift '0'
→ Largest Bandwidth		→

Applications:-

- → constant Current Source
- → High frequency Amplifier
- → As a Non-inverting Voltage Amplifier
- → As a impedance matching device.

- → Amplification purpose

- → Audio freq. Power Amplifier
- → As a Buffer.
- → cc amplifier also called as "Emitter follower".

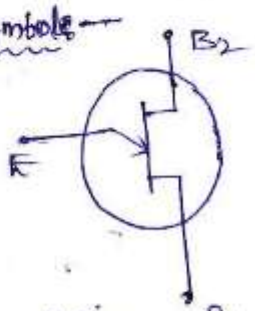
UJT [Uni Junction Transistor]:-

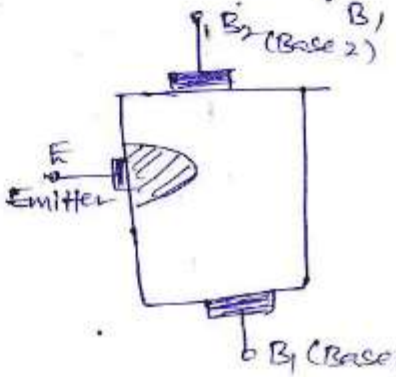
→ UJT is a three terminal semiconductor switching device.

→ It has only one PN Junction and three leads, it is commonly called as "Uni-Junction Transistor".

→ It consists of a lightly doped N-type silicon bar with a heavily doped p-material alloyed to its one side nearer to Base 2 for producing single PN Junction.

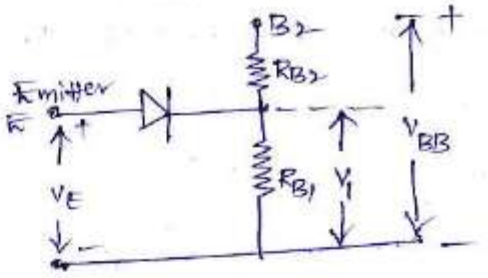
Symbole:-





Characteristics of UJT:

The interbase resistance between Base2 and Base1 of the bar is $R_{BB} = R_{B1} + R_{B2}$.



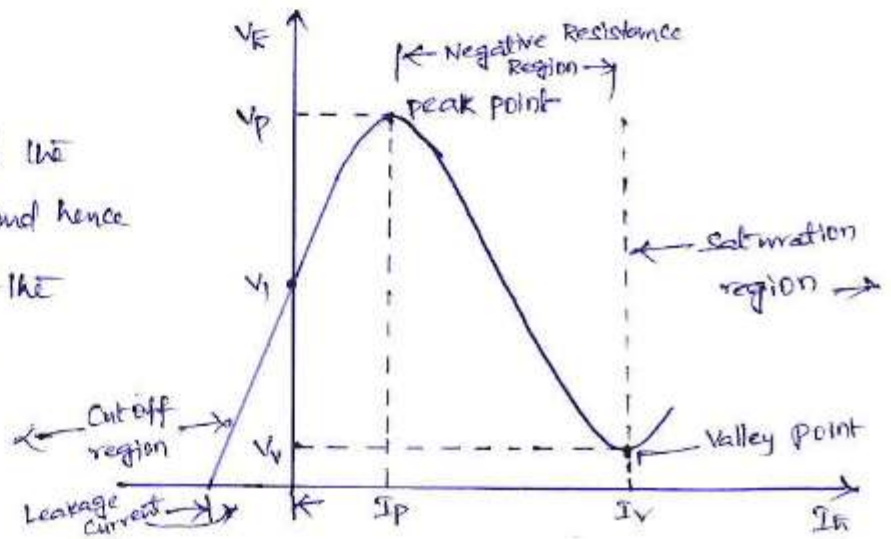
With Emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the N-type bar. The voltage drop across R_{B1} is given by $V_1 = \eta V_{BB}$ where η is the intrinsic stand off ratio and is equalent to $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}$.

The typical value of η ranges from 0.56 to 0.75. This voltage V_1 reverse biases the PN Junction and I_E is Cut-off. But a small leakage Current flows from Base2 to Emitter due to minority Carriers.

→ If a positive voltage V_E is applied to the emitter the P-N Junction will remain in reverse biased as long as V_E is less than V_1. If V_E exceeds V_1 by the cut in voltage V_γ, the diode becomes forward Biased. under this condition holes are injected into N-type bar. These holes are repelled by the terminal B_2 and are attracted by the terminal B_1. Accumulation of holes in Emitter to Base1 region reduces the resistance in this section and hence I_E is increased and is limited to V_E. The device is now in the ON state.

→ If a negative voltage is applied to the Emitter, PN Junction remains reverse biased and the I_E is Cutoff. The device is now in the off state.

→ Upto the peak point 'P', the diode is reverse biased and hence the region to the left of the Peak point 'P', the diode is reverse biased and hence the region to the left of



peak point is called 'Cut-off region'.

→ The UJT has a stable firing voltage 'V_p' which depends on V_{BB} & I_p.

→ At P, the $V_p = \eta V_{BB} + V_\gamma$, the diode starts conducting and holes are injected into N-layer. Hence resistance decreases there by decreasing V_E for the increase in I_E. There is a negative resistance region from peak point 'p' to valley point 'v'.

After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN Junction Diode.

→ The region to the right of the valley point is called 'saturation region'.

→ At the valley point, the resistance changes from negative to positive.

→ for very large I_E, the characteristics asymptotically approaches the curve for $I_{B2} = 0$.

→ A unique characteristic of UJT is when it is triggered then the I_E increases regeneratively untill it is limited by emitter power supply.

→ Due to negative resistance property, UJT can be employed in a variety of applications viz sawtooth wave generator, pulse generator, switching purpose, timing and control circuits.

Biasing and stabilization:—

In order to produce distortion free output in amplifier circuits the supply voltage and resistances in the circuit must be suitably chosen. These voltages and resistances establish a set of dc voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called "Quiescent values". which determine the operating point for the transistor.

→ The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called "Biasing".

→ The circuits used for getting the desired and proper operating point are known as "Biasing circuits".

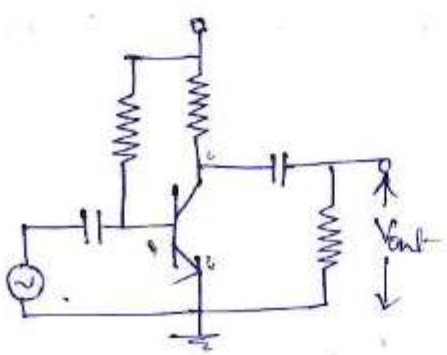
→ Operating point:—

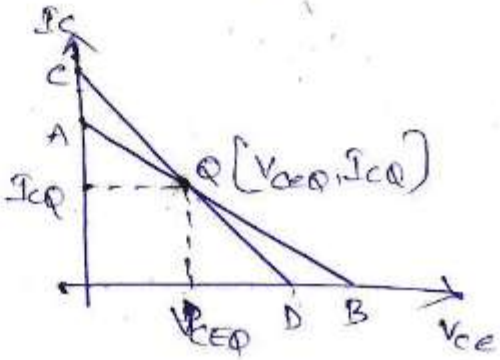
operating point or Q-point [Quiescent point] is the point at which the transistor is operating as an amplifier.

The Quiescent point changes with temperature. But Q-point must be fixed otherwise it produces distorted output.

→ It is very essential to choose the operating point properly so that the transistor is operated in the active region and that the operating point doesnot change with temperature. operating point is fixed with respect to the output characteristic of a transistor only.

→ for the common-emitter transistor configuration,





Since in Common ~~Emitter~~ Amplifier Configuration, By applying KVL to the collector circuit

$$V_{cc} - I_c R_c - V_{ce} = 0 \Rightarrow \boxed{V_{cc} = I_c R_c + V_{ce}}$$

Since the values of V_{cc} and R_c are fixed and I_c and V_{ce} are depends on R_B.

from the above equation we can draw the DC load line. The The coordinates of the end points are obtained by substituting $V_{ce} = 0$ and $I_c = 0$ individually.

→ End point 'A' can be obtained by substituting $V_{ce} = 0$ in the above equation. Therefore the coordinates of 'A' are $V_{ce} = 0$ and $i_c = V_{cc}/R_c$.

→ The coordinates of B are obtained by substituting $i_c = 0$ in the above equation. Then $V_{ce} = V_{cc}$. Therefore the coordinates of 'B' are $V_{ce} = V_{cc}$ and $I_c = 0$. Thus the line joining the coordinates of 'A' and 'B' gives the DC load line. Thus the DC load line AB can be drawn if R_c and V_{cc} are known.

→ The optimum Q-point is located at the mid point of the dc load line AB between the Saturation and Cut off regions i.e. Q is exactly midway between A & B. In order to get faithful amplification, Q-point must be well with in the active region of the transistor.

→ Even though the Q-point is fixed properly, it is very important to ensure that the operating point remains stable when it is originally fixed. If the Q-point shifts nearer to either A or B the output voltage and current get clipped, there by output signal is distorted.

→ In practice, Q-point tends to shift its position due to any or all of the following three main factors. They are

(1) Reverse saturation Current (I_{CO}) doubles for every 10°C rise in temperature.

(ii) V_{BE} decreases by 2.5 mV/°C.

(iii) Transistor Current gain 'β', which increases with temperature.

The base Current is kept constant since I_B is approximately equal to V_{CC}/R_B.

→ If the transistor is replaced by another one of the same type, parameters are not identical. parameters such as β vary over a range: This results in a variation of I_C for a given I_B. Hence in the output characteristics, the spacing between the curves might increase or decrease which leads to the shift of the Q-point to a location which might be completely unsatisfactory.

AC Load Line: —

After drawing DC Load line, the operating point 'Q' is properly located at the Centre of the DC load line. This operating point is chosen under zero input signal condition of the circuit. Hence the AC Load line should also pass through the operating point 'Q'. The effective AC Load resistance R_{ac} is the combination of R_C parallel to R_L i.e., $R_{ac} = R_C \parallel R_L$. So the slope of the ac load line CQD will be $(-1/R_{ac})$.

→ To draw the AC Load line, two end points viz. Maximum of V_{ce} and Max. I_C when the signal is applied are required.

→ Maximum $V_{ce} = V_{CEQ} + I_{CQ}R_{ac}$. which locates the point D (OD) on the V_{ce} axis. Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C(oc) on the I_C axis.

By Joining points 'c' and D, ac load line CD is constructed. As $R_C < R_{ac}$, the DC Load line is less steep than the ac load line.

→ When the signal is zero, we have the exact DC conditions. The intersection of DC and AC Load lines are at the Operating point 'Q'.

Need for Biasing :—

→ Biasing is the process of giving proper supply voltages and resistances for obtaining the desired operating point.

To maintain the operating point at a stable position we need a Biasing. If the operating point is stable in such case only proper amplification may takes place. Otherwise the signal is distored if the operating point is not at stable position.

→ Various Biasing circuits used to maintain the operating point at stable position are

(i) fixed Bias Circuit [Base Bias Circuit]

(ii) Collector to Base Bias Circuit [collector feedback Bias]

(iii) Self Bias or Emitter Bias Circuit.

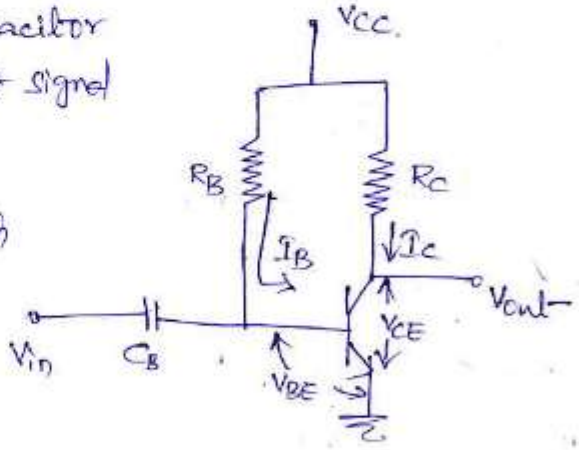
fixed Bias Circuit :— (or Base Resistor Method)

Consider the NPN transistor circuit shown in figure below.

Capacitor Blocks DC since the capacitor is open circuit for DC. So the output signal will be pure ac signal.

R_C is the Collector Resistance. which limits the Current I_C.

R_B provides the bias voltage for the base.



By applying KVL to the base circuit,

$$V_{cc} - I_B R_B - V_{BE} = 0 \Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

Since $V_{BE} = 0.2V$ for Ge, $V_{BE} = 0.6$ for Si.

→ In order to get a large value of I_B or the change in the operating point, V_{cc} or R_B has to be changed. Since once V_{cc}, R_B etc are fixed I_B is fixed. So the above circuit is called "fixed Bias Circuit".

I_B is fixed when V_{cc} and R_B are fixed. Because in the expression for I_B, β is not appearing. So once R_B and V_{cc} are fixed the biasing point is also fixed. Hence the name "fixed Bias Circuit".

Stability factor:—

The extent to which the collector current I_c is established with varying I_{co} is measured by a stability factor 'S'.

→ It is defined as the rate of change of collector current I_c with respect to the collector base leakage current I_{co}, keeping both the current I_B and the current gain β constant.

$$S = \frac{\partial I_c}{\partial I_{co}} \equiv \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant.}$$

Since the collector current for a CE amplifier is given by

$$I_c = \beta I_B + (\beta+1) I_{co}$$

where I_B depends on Base & collector Resistances.

I_B is constant since R_B and R_c are fixed. 'β' is same for a transistor.

Differentiating the above equation with respect to I_c, we get

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (\beta+1) \frac{\partial I_{co}}{\partial I_c}$$

Therefore, $$\left(1 - \beta \frac{\partial I_B}{\partial I_c}\right) = (\beta+1) \frac{\partial I_{co}}{\partial I_c} = \underbrace{(\beta+1)}_{S}$$

$$\therefore \boxed{S = \frac{(1+\beta)}{1 - \beta\left(\frac{\partial I_B}{\partial I_c}\right)}}$$

From this equation, it is clear that this factor 'S' should be small as possible to have better thermal stability.

Stability factors S' and S'':—

→ The stability factor 'S' is defined as the rate of change of I_C with V_{BE}, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \cong \frac{\Delta I_C}{\Delta V_{BE}}$$

→ The stability factor 'S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\Delta \beta}$$

*→ for a fixed Bias Circuit,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \longrightarrow (1)$$

Since stability factor $(S) = \dfrac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$

from eqn (1),

$$\frac{\partial I_B}{\partial I_C} = 0 \quad [\because V_{CC} \text{ & } V_{BE} \text{ are fixed}]$$

$$\therefore S = \frac{1+\beta}{1-\beta(0)} = 1+\beta.$$

***

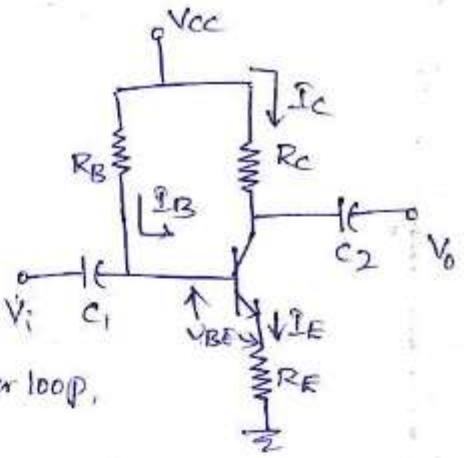
$S = 1+\beta$ for fixed Bias Circuit

Since β is a large quantity, so this is a very poor bias stable circuit. Therefore, in practice, this circuit is not used for biasing the base.

→ The advantage of this method are: (a) Simplicity (b) Small number of components required. (c) [illegible] supply voltage

Emitter feedback Bias :—

The Emitter-feedback bias network contains an emitter resistor for improving the stability level over that of fixed bias configuration.



→ By Applying KVL for the base feedback emitter loop, we get

$$V_{cc} - i_B R_B - V_{BE} - I_E R_E = 0$$

$$\because I_E = I_B + I_C$$

$$\therefore V_{cc} - i_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$\Rightarrow V_{cc} - i_B(R_B + R_E) - V_{BE} - i_C R_E = 0 \Rightarrow V_{cc} - V_{BE} = I_B(R_B + R_E) + I_C R_E$$

Therefore, $$I_B = \frac{V_{cc} - V_{BE}}{R_E + R_B} - \left(\frac{R_E}{R_E + R_B}\right) I_C$$

Here V_{BE} is independent of I_C.

Hence, $$\frac{\partial I_B}{\partial I_C} = -\left(\frac{R_E}{R_E + R_B}\right)$$

Since, we know that: $$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

$$\therefore S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_E+R_B}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

Since $1 + \frac{\beta R_E}{R_E + R_B} > 1$, $S < (1+\beta)$.

From this the value of the stability factor S is always lower in Emitter-feedback bias circuit than that of fixed bias circuit.

→ By applying KVL for the collector Emitter loop, we get

$$V_{cc} - I_C R_C - V_{ce} - I_E R_E = 0$$

$$\because I_E = I_C + I_B$$

$$V_{cc} - I_C[R_C + R_E] - V_{ce} = 0$$

$I_E \approx I_C$, $\because I_B$ is very small.

and $$V_{cc} = V_{ce} + I_C[R_C + R_E]$$

V_E is the voltage from Emitter to ground and is determined by

$$V_E = I_E R_E$$

The voltage from collector to ground can be determined from

$$V_{ce} = V_C - V_e$$

and $V_C = V_{ce} + V_e$ or $V_C = V_{cc} - I_C R_C$

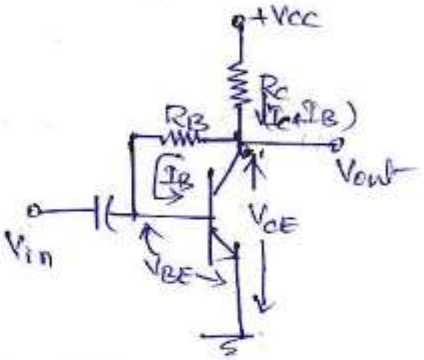
The voltage at the base with respect to ground can be determined from

$$V_B = V_{cc} - I_B R_E$$

(or) $V_B = V_{BE} + V_E$

Collector to Base Bias (or collector feedback Bias):—

→ This circuit is shown in figure. This circuit is the simplest way to provide some degree of stabilization to the amplifier operating point.



→ If the collector current I_C tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher β, the voltage drop across R_C increases, thereby reducing the value of V_{ce}. Therefore, I_B decreases which, in turn, compensates the increase in I_C. Thus greater stability is obtained.

By applying KVL to the Base circuit,

$$V_{cc} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0 \Rightarrow V_{cc} - I_C R_C - (R_B + R_C) I_B - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{cc} - V_{BE} - I_C R_C}{(R_B + R_C)}$$

Therefore, $$\frac{dI_B}{dI_C} = \frac{-R_C}{(R_B+R_C)} \frac{\partial I_C}{\partial I_C} = \frac{-R_C}{R_B+R_C}$$

Since stability factor, $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$

$$\therefore \boxed{S = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_B+R_C}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}}$$

The value of 'S' is smaller than the value obtained by fixed bias circuit.

. The stability factor 'S' can be improved by making R_B small or R_C large.

→ If R_C is very small, then $S = \beta + 1$ i.e., stability is very poor. Hence the value of R_C must be quite large for good stabilization. Thus collector to base bias arrangement is not satisfactory for the amplifier circuits like transformer coupled trans amplifier, where the dc load resistance in collector circuit is very small. for such amplifiers, emitter bias or self bias will be the most satisfactory transistor for stabilization.

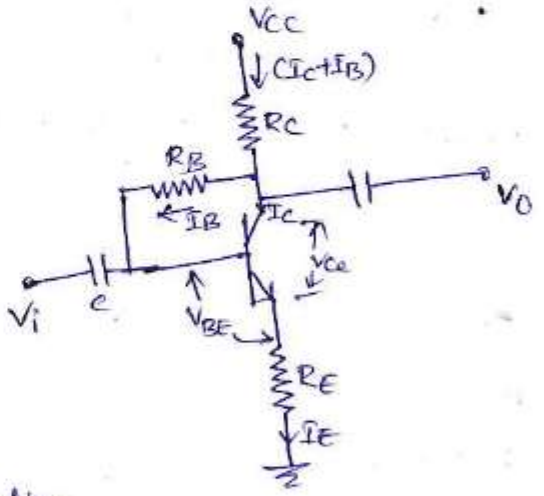
→ If R_B small & R_C large.

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C}\right)} = \frac{1+\beta}{1+\beta} = 1$$

in this case, stability is more.

Collector - Emitter feedback Bias:-

This circuit can be obtained by applying both the collector feedback and emitter feedback.



Here the collector feedback is provided by connecting a resistance R_B from the collector to base and emitter feedback is provided by connection an emitter resistance R_E from the Emitter to ground. Both the feedbacks are used to control the Current I_B [Base Current] and I_C [collector Current] in the opposite direction to increase the stability. as

→ By applying KVL to the base circuit,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\because I_E = I_B + I_C$$

$$\therefore V_{CC} - [I_C + I_B]R_C - I_B R_B - V_{BE} - [I_B + I_C]R_E = 0$$

Therefore, $I_B = \frac{V_{CC} - V_{BE}}{R_E + R_C + R_B} - \left(\frac{R_E + R_C}{R_E + R_C + R_B}\right) I_C$

Since V_{BE} is independent of I_C,

$$\boxed{\frac{\partial I_B}{\partial I_C} = -\left(\frac{R_E + R_C}{R_E + R_C + R_B}\right)}$$

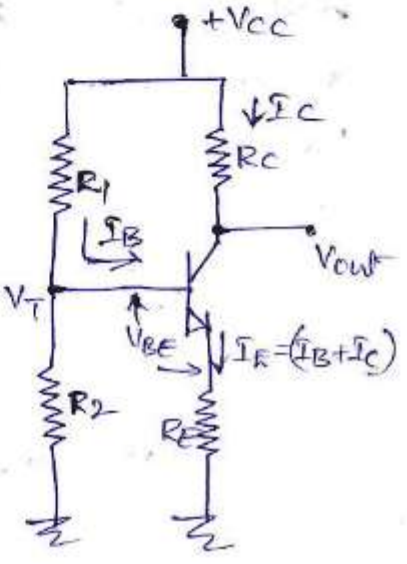
Since $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$

$$\therefore \boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_E + R_C}{R_E + R_C + R_B}\right)}}$$

From this, it is clear that the stability factor of the collector - Emitter feedback bias circuit is always better than that of the collector feedback and emitter feedback circuits.

Emitter Bias (or) Self Bias (or) Voltage Divider Bias :— (or) potential Divider Bias :

Potential Divider circuit can be used for low collector resistance. The current in the emitter resistor R_E causes a voltage drop which is in the direction to reverse Bias the emitter junction.

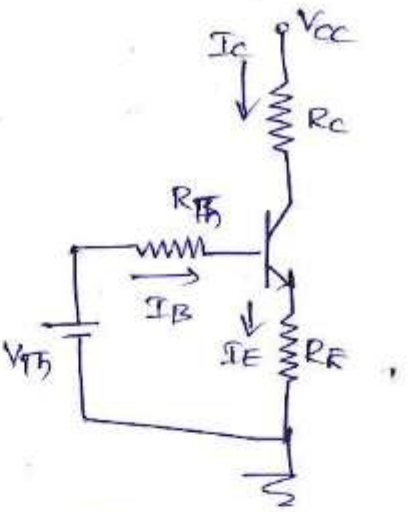


for the transistor to remain in the active region, the base emitter junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistances R_1 and R_2.

⑥ Stability factor 'S' :—

By applying Thevenin's Theorem to the input-ss base circuit, for finding the base Current, we have,

$$V_T = \frac{R_2 V_{cc}}{R_1+R_2} \quad \text{and} \quad R_{Th} = \frac{R_1 R_2}{R_1+R_2}$$



Thevenin's equivalent circuit

The loop equation around the base circuit can be written as

$$V_T = I_B R_{Th} + V_{BE} + (I_B + I_C) R_E$$

Differentiating the above eqn w.r.t I_C, we get

$$0 = \frac{\partial I_B}{\partial I_C} R_{Th} + \frac{\partial I_B}{\partial I_C} R_E + R_E \Rightarrow \left(R_{Th}+R_E\right)\frac{\partial I_B}{\partial I_C} = -R_E$$

$$\therefore \boxed{\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E+R_{Th}}}$$

Since

$$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_{Th}}\right)}$$

Therefore,

$$S = \frac{(1+\beta)(R_E+R_{Th})}{R_E+\beta R_E+R_{Th}} = \frac{(1+\beta)R_E\left[1+\frac{R_{Th}}{R_E}\right]}{R_E\left[1+\beta+\frac{R_B}{R_E}\right]} = \frac{(1+\beta)\left[1+\frac{R_{Th}}{R_E}\right]}{1+\beta+\frac{R_{Th}}{R_E}}$$

$$\boxed{S = (1+\beta)\,\frac{1+\frac{R_{Th}}{R_E}}{1+\beta+\frac{R_{Th}}{R_E}}}$$

from the above equation, the value of stability factor 'S' is unity when Thevenins Base resistance is very small than the Emitter Resistance.

→ if Emitter Resistance (R_E) is zero then the stability factor goes on increasing till $S = 1+\beta$.

The stability factor value equal to 1 is achieved at the cost of power dissipation.

→ To improve the stability, the equivalent resistance R_{Th} must be decreased

To determine the stability factor(S'):

$$S' = \frac{\partial I_C}{\partial V_{BE}}\Big|_{I_{CO}\,\&\,\beta\ \text{constant}} = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$\because V_T = I_B R_{BB} + V_{BE} + I_E R_E$$

$$= I_B[R_{BB} + R_E] + I_C R_E + V_{BE} \quad [\text{Since } I_E = I_B + I_C]$$

But we have $I_C = \beta I_B + (1+\beta) I_{CO}$

$$\therefore I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta}$$

$$\therefore V_T = \frac{I_C}{\beta}[R_{BB} + R_E] + V_{BE} + I_C R_E + \left(\frac{1+\beta}{\beta}\right)[R_{BB} + R_E] I_{CO}$$

Differentiating the above equation w.r.t V_{BE}, we get

$$0 = \frac{\partial I_C}{\partial V_{BE}}\left(\frac{R_{BB} + R_E}{\beta}\right) + 1 + R_E \frac{\partial I_C}{\partial V_{BE}} + 0 \Rightarrow -1 = \frac{\partial I_C}{\partial V_{BE}}\left[R_E + \frac{R_E + R_{BB}}{\beta}\right]$$

$$\Rightarrow \frac{\partial I_C}{\partial V_{BE}}\left[\frac{R_{BB} + (1+\beta) R_E}{\beta}\right] = -1 \Rightarrow \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_{BB} + (1+\beta) R_E}$$

$$\therefore \boxed{S = \frac{-\beta}{R_{BB} + (1+\beta) R_E}}$$

To determine the stability factor(S''):

Since $S'' = \frac{\partial I_C}{\partial \beta}\Big|_{I_{CO},\,\beta = \text{constant}}$

$$I_C = \frac{\beta(V_T - V_{BE})}{R_{BB} + (1+\beta) R_E} + \frac{\beta\left(\frac{1+\beta}{\beta}\right) I_{CO}(R_{BB} + R_E)}{R_{BB} + (1+\beta) R_E}$$

Since $\beta >> 1$,

numerator of II term can be written as

$$(R_{BB} + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} \simeq (R_{BB} + R_E) I_{CO}$$

$$\therefore I_C = \frac{\beta(V_T - V_{BE})}{R_{BB} + (1+\beta) R_E} + \frac{\beta(R_{BB} + R_E) I_{CO}}{R_{BB} + (1+\beta) R_E}$$

therefore, $$I_C = \frac{\beta[V_T - V_{BE} + (R_{BB} + R_E) I_{CO}]}{R_{BB} + (1+\beta) R_E}$$

Let $V' = (R_{B} + R_E) I_{CO}$

Therefore, $I_C = \frac{\beta[V_T - V_{BE} + V']}{R_B + (1+\beta) R_E}$

Differentiating above eqn w.r.t 'β' and then simplifying

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta\left[1 + \beta\left(\frac{R_E}{R_E + R_B}\right)\right]} = \frac{S I_C}{\beta(1+\beta)}$$

$$\boxed{S'' = \frac{S I_C}{\beta(1+\beta)}}$$

** If I_C tends to increase, due to increase in I_{CO} with temperature the current in R_E increases. Hence the voltage drop across R_E increases there by decreasing the base current. As a result, I_C is maintained almost constant. So self bias circuit is used as constant current circuit.

→ Self Bias also called 'potential devider Bias circuit' or 'emitter Bias circuit".

→ It is the most popularly used biasing circuit.

→ The advantages of using emitter resistance are
(i) Input resistance increases by a larger value.
(ii) It provides stabilization.

→ The disadvantage of using emitter Resistance is, it introduces negative feed back. Therefore it reduces the voltage gain.

→ R_1 and R_2 are called "Biasing resistors' and they are used to provide a base current into the transistor.

→ R_1 and R_2 are in parallel and both must be in K-Ω's or hundreds of KΩ's.

→ $R_1 >> R_2$, otherwise $R_1 \geq 10 R_2$.

Stabilization against variations in V_{BE} and β :—

Equation for R_1 & R_2 for the self Bias circuit :—

Since $V_{Th} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} \rightarrow (1)$, $R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \rightarrow (2)$

$(1)/(2) \Rightarrow \frac{V_{Th}}{R_{Th}} = \frac{V_{CC}}{R_1} \Rightarrow \boxed{R_1 = \frac{V_{CC} \cdot R_{Th}}{V_{Th}}}$

Substitute 'R_1' in eqn (2), then

$$R_{Th} = \frac{\frac{V_{CC} \cdot R_{Th}}{V_{Th}} \times R_2}{\frac{V_{CC} R_{Th}}{V_{Th}} + R_2} \Rightarrow R_{Th} = \frac{V_{CC} \cdot R_{Th} \cdot R_2}{V_{CC} R_{Th} + V_{Th} \cdot R_2}$$

$$\Rightarrow V_{CC} R_{Th} + V_{Th} \cdot R_2 = V_{CC} \cdot R_2$$

$$\Rightarrow V_{CC} R_{Th} = (V_{CC} - V_{Th}) R_2 \Rightarrow \boxed{R_2 = \left(\frac{V_{CC}}{V_{CC} - V_{Th}}\right) R_{Th}}$$

Stabilization against Variations in V_{BE} and β :—

→ Using P-N Junctions diodes, compensation is done for V_{BE} and I_{CO}

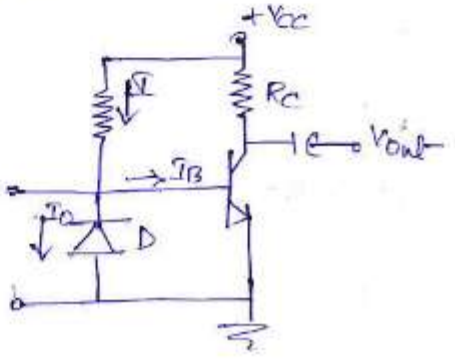
Bias compensation :—

The collector to base bias circuit and self bias circuit are used for stability of I_C with variation in I_{CO}, V_{BE} and β. But there is feed back from the output to the input. Hence the amplification will be reduced, even though the stability is improved.

→ If the reduction in gain is not tolerable then Compensation techniques are tobe used. Thus both stabilization and compensation technique are used depending upon the requirements.

Diode Compensation for I_{CO}, V_{BE} :—

(i) figure shows a transistor amplifier with a Diode is connected across the base emitter Junction for Compensation of change in collector saturation Current I_{CO}.



The Diode is of the same material as the transistor and it is reverse biased by the base-emitter junction voltage (V_{BE}), allowing the diode reverse saturation Current I_o to flow through Diode D. The base Current $I_B = I - I_o$.

→ As long as temparature is constant, Diode D operates as a resistor. As temparature increases, I_{Co} of the transistor increases. Hence to Compensate for this, the base Current 'I_B' should be decreased.

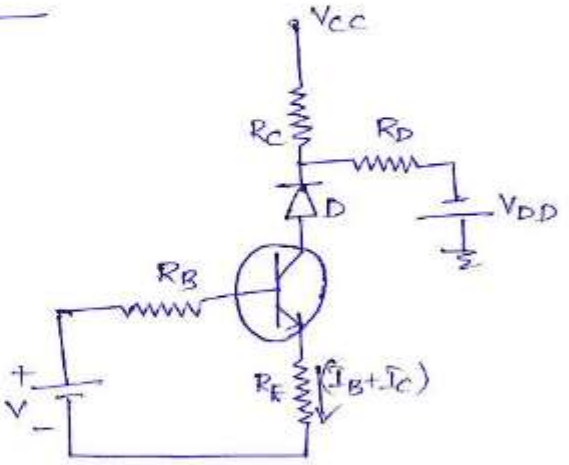
→ The increase in temparature will also cause the leak Current I_o through D to increase and there by decreasing the base Current I_B. This is the required action to keep I_c constant.

→ This method of bias Compensation doesnot need a change in I_c to effect the change in I_B as both I_{Co} and I_o can track almost equally according to the change in temp°.

(ii) Diode Compensation for V_{BE} :-

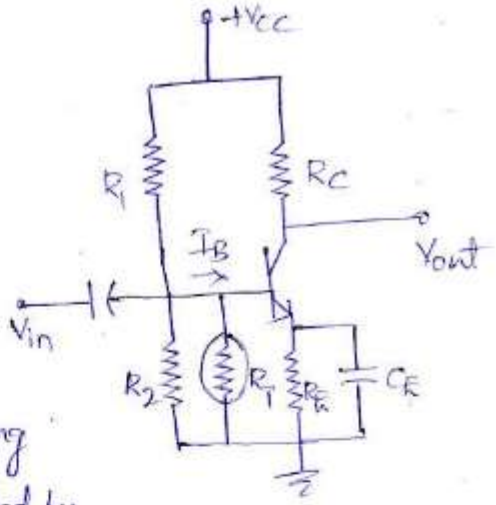
The circuit shown in figure 8 employs self biasing technique for stabilization. In addition a diode is connected in the emitter circuit and it is forward biased by the Source V_{DD}. Resistance R_d limits the Current through the diode. The diode should be of the same material as the transistor. The negative voltage 'V_D' across the diode will have the same temparature coefficient as V_{BE}. Since the Diode is connected as shown, if V_{BE} decreases with increase in temparature [V_B is Cut-in Voltage], V_D increases with temp°. Since with temp°, the mobility of Carriers increases, so Current through the diode increases and V_D increases. Therefore, as V_{BE} decreases, V_D increases. So that I_c will be insensitive to variations in V_{BE}.

The decrease in V_{BE} is nullified by Corresponding increase in V_D. So the net voltage more or less remains constant. Thus the diode Circuit Compensates for the changes in the values of V_{BE}.



Thermistor Compensation:

A thermistor, R_T, having a negative temparature coefficient is connected in parallel with R_2. The resistance of thermistor decreases exponentially with increase of temparature. An increase in temparature will decrease the base voltage V_{BE}, reducing I_B and I_C. Bias stabilization is also provided by R_E and C_E.



Thermal Runaway:

The collector Current for the CE circuit is given by

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

The three variables in the equation, β, I_B and I_{CO} increase with rise in temparature. In particular, the reverse saturation Current or leakage Current I_{CO} changes greatly with temperature. specifically it doubles for every 10°C rise in temparature. The collector Current I_C causes the collector base junction temperature to rise which, in turn, increase I_{CO}, as a result I_C will increase still further, which will further rise the temparature at the collector-base junction. This process will become cumulative leading to 'Thermal Runaway'. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

→ If the circuit is designed such that the base Current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for the increase in $(1+\beta) I_{CO}$, keeping I_C almost constant.

Thermal stability :—

As the temparature changes I_{CO} changes then I_C changes. I_C causes the collector base junction temparature to rise which inturn increase I_{CO} and the process continues. Consequently the transistor are exceeded which may destroy the transistor itself. Inorder to prevent this the device must be stable thermally.

Condition for Thermal stability :—

For preventing thermal runaway, the required condition is that the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence, the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \longrightarrow (1)$$

In the self bias circuit, the transistor is biased in the Active region. The power generated at the collector junction without any signal is

$$P_C = I_C V_{CB} = I_C V_{CE} \longrightarrow (2)$$

Let us assume that the Quiescent collector and Emitter Currents are equal. Then $P_C = I_C V_{CC} - I_C^2 (R_E + R_C) \longrightarrow (3)$

The condition to prevent thermal runaway can be rewritten as

$$\frac{\partial P_C}{\partial I_C} \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \longrightarrow (4)$$

As θ and $\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}$ should be negative inorder to satisfy the above Condition.

Differentiating eqn(3) w.r.t. I_C, we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_E + R_C) \longrightarrow (5)$$

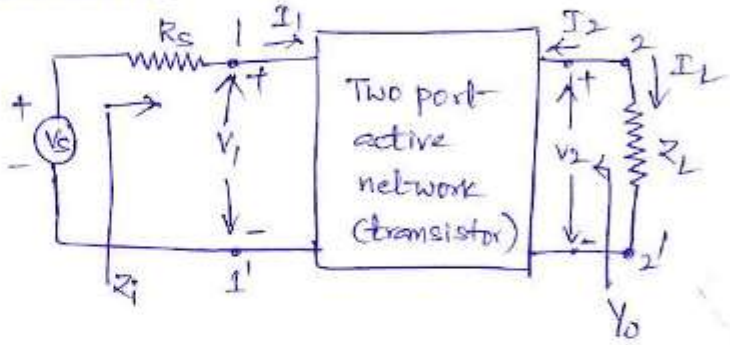
Hence, to avoid thermal runaway, it is necessary that

$$\boxed{I_C > \frac{V_{CC}}{2(R_E + R_C)}} \longrightarrow (6)$$

Since $V_{CE} = V_{CC} - I_C(R_E + R_C)$ then eqn(6) implies that $V_{CE} < V_{CC}/2$. If the inequality of eqn(6) is not satisfied and $V_{CE} < V_{CC}/2$, then from eqn(5), $\frac{\partial P_C}{\partial I_C}$ is positive, and corresponding eqn(4) should be satisfied, otherwise thermal runaway will occur.

Analysis of a Transistor Amplifier Circuit using h-parameters:

The hybrid equivalent circuit is valid for any type of load whether it is pure resistive or impedance or another transistor. It is assumed that h-parameters remain constant over the operating range. further, the input is sinusoidal and V_1, I_1, V_2 and I_2 are phasor quantities.

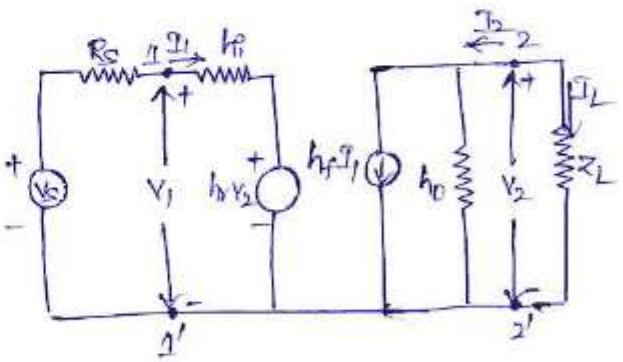


Current Gain (or)

Current Amplification (A_I):

Current Gain A_I is defined as the ratio of output current to input current i.e.,

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$



From the circuit, By KVL at the output

$$I_2 = h_f I_1 + h_o V_2$$

By substituting, $V_2 = I_L Z_L = -I_2 Z_L$,

$$\therefore I_2 = h_f I_1 - I_2 Z_L h_o$$

$$\therefore I_2 + Z_L h_o I_2 = h_f I_1 \Rightarrow I_2[1 + Z_L h_o] = h_f I_1$$

$$\therefore \boxed{A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}}$$

Input Impedance (Z_i):-

In the circuit, R_s is the signal source resistance. The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Z_i, i.e.,

$$Z_i = \frac{V_1}{I_1}$$

From the circuit, $V_1 = h_i I_1 + h_r V_2$

Hence, $$Z_i = \frac{h_i I_1 + h_r V_2}{I_1} = h_i + h_r \frac{V_2}{I_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$Z_i = h_i + h_r \frac{A_I I_1 Z_L}{I_1}$$

resulting in $$\boxed{Z_i = h_i + h_r A_I Z_L}$$

Since $$A_I = \frac{-h_f}{1+h_o Z_L}$$

$$\therefore Z_i = h_i - \frac{h_f h_r Z_L}{1+h_o Z_L} = h_i - \frac{h_f h_r Z_L}{Z_L[h_o + Y_{Z_L}]}$$

By taking the load admittance as $Y_L = Y_{Z_L}$.

$$\boxed{Z_i = h_i - \frac{h_f h_r}{h_o + Y_L}}$$

The input impedance is a function of load impedance.

Voltage Gain (or) Voltage Amplification factor (A_V):-

The ratio of output voltage V_2 to input voltage V_1 gives the voltage gain of the transistor, i.e.,

$$A_V = \frac{V_2}{V_1}$$

Substituting, $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

$$\boxed{A_V = \frac{A_I Z_L}{Z_i}}$$

Output Admittance (Y_o):

By definition, Y_o is obtained by setting V_s to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current drawn from V_2 is I_2, then

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0 \text{ and } R_L = \infty.$$

from the circuit, $I_2 = h_f I_1 + h_o V_2$

By dividing with V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$ ——→ (a)

With $V_s = 0$, by KVL in input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1 (R_s + h_i) + h_r V_2 = 0 \Rightarrow I_1 [R_s + h_i] = -h_r V_2$$

Hence, $\frac{I_1}{V_2} = \frac{-h_r}{h_i + R_s}$ ——→ (b)

By substituting eqn(b) in eqn(a), then

$$\frac{I_2}{V_2} = \frac{-h_f h_r}{h_i + R_s} + h_o$$

$$\therefore \boxed{Y_2 = h_o - \frac{h_f h_r}{h_i + R_s}}$$

From the above equation, the output admittance is a function of source resistance.

If the source impedance is resistive then Y_o is real.

Voltage Amplification (A_{vs}) taking into Account the resistance (R_s) of the Source:

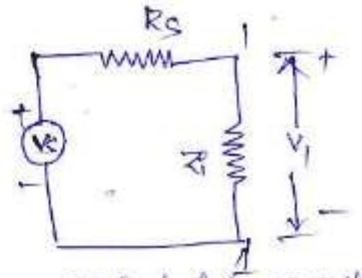
The overall voltage gain (A_{vs}) is given by

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_s} = A_v \cdot \frac{V_1}{V_s}$$

From Thevenins equivalent at the input

$$V_1 = \frac{V_s Z_i}{Z_i + R_s} \Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s}$$

Then $\boxed{A_{vs} = A_v \frac{Z_i}{Z_i + R_s}}$



Equivalent i/p circuit

Since $A_V = \frac{A_I Z_L}{Z_i}$

$$\therefore \boxed{A_{VS} = \frac{A_I Z_L}{Z_i + R_S}}$$

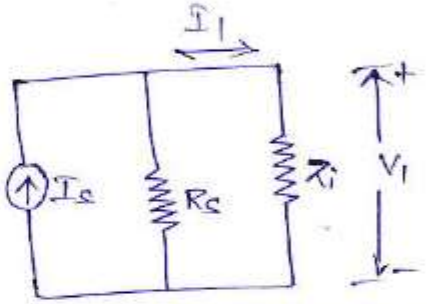
If $R_S = 0$, then $A_{VS} = \frac{A_I Z_L}{Z_i} = A_V$. Hence A_V is the voltage gain with an ideal voltage source.

Current Amplification (A_{IS}) taking into account the Source Resistance(R_S)

The overall Current Gain,

$$A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} * \frac{I_1}{I_S} = A_I \frac{I_1}{I_S}$$

$$\boxed{A_{IS} = A_I \frac{I_1}{I_S}}$$



Equivalent Input Circuit

from Norton's Equivalent at the input,

$$I_1 = I_S \cdot \frac{R_S}{R_S + Z_i}$$

$$\therefore \frac{I_1}{I_S} = \frac{R_S}{R_S + Z_i}$$

and hence, $$\boxed{A_{IS} = A_I \cdot \frac{R_S}{R_S + Z_i}}$$

If $R_S = 0$, then $A_{IS} = A_I$.

$A_I \rightarrow$ Current Gain with an ideal Current Source.

$$\therefore A_{VS} = \frac{A_I Z_L}{Z_i + R_S} \cdot \frac{R_S}{R_S}$$

then $$\boxed{A_{VS} = \frac{A_{IS} Z_L}{R_S}}$$

Power Gain (A_P):—

→ Average power delivered to the load is $P_2 = |V_2||I_L| \cos\theta$ where θ is the phase angle between V_2 and I_L. Assume that Z_L is resistive i.e., $Z_L = R_L$. Since h-parameters are read at low frequencies, the power delivered to the load is $P_2 = V_2 I_L = -V_2 I_2$.

Since the input power $P_i = V_i I_i$, the operating power gain A_p of the transistor is defined as,

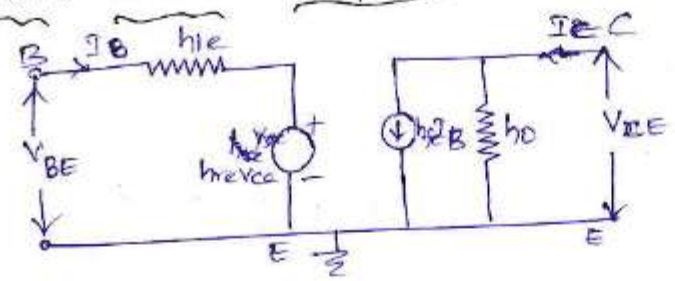
$$A_p = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V \cdot A_I = A_I \cdot A_I \frac{R_L}{R_i'}$$

$$\boxed{A_p = A_I^2 \left[\frac{R_L}{R_i'}\right]}$$

	Common Base	Common Emitter	Common Collector
Current Gain (A_I)	$\frac{-h_{fb}}{1+h_{ob}R_L}$	$A_I = \frac{-h_{fe}}{1+h_{oe}R_L} \approx -h_{fe}$ $[h_{oe}R_L < 0.1]$	$A_I = \frac{-h_{fc}}{1+h_{oc}R_L}$
Input Impedance (R_i)	$R_i = h_{ib} + h_{rb}A_I R_L$	$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}+Y_{RL}}$	$R_i' = h_{ic} + h_{rc}A_I R_L$
Voltage Gain (A_V)	$A_V = \frac{A_I R_L}{R_i}$	$A_V = A_I \cdot \frac{R_L}{R_i'}$	$A_V = A_I \frac{R_L}{R_i}$
Output Resistance (R_o)	$R_o = 1/Y_o$ where $Y_o = h_{ob} - \frac{h_{fb}h_{rb}}{h_{ib}+R_s}$	$R_o = 1/Y_o$ where $Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}+R_s}$	$R_o = 1/Y_o$ where $Y_o = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ic}+R_s}$

EDC
IV (12)

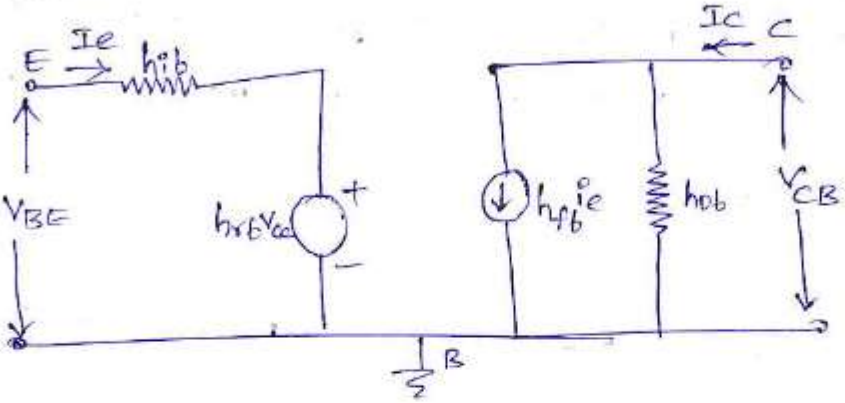
Common Emitter Amplifier:-



$V_{BE} = h_{ie} i_b + h_{re} V_{ce}$

$i_c = h_{fe} i_b + h_{oe} V_{ce}$

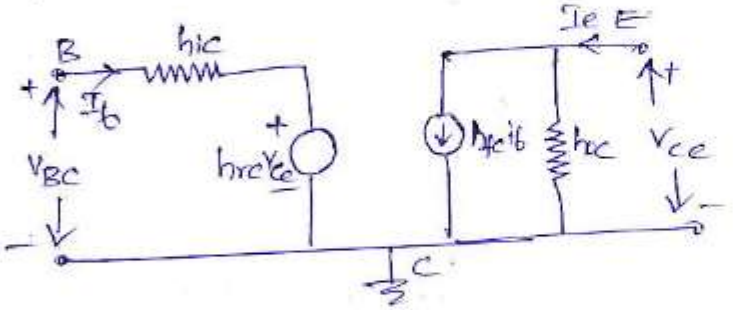
Common Base Amplifier:-



$V_{EB} = h_{ib} i_e + h_{rb} V_{cb}$

$i_c = h_{fb} i_e + h_{ob} \cdot V_{cb}$

Common Collector Amplifier:-



$V_{BC} = h_{ic} i_b + h_{rc} \cdot V_{ce}$

$i_e = h_{fc} i_b + h_{oc} \cdot V_{ce}$

Comparison of Transistor Amplifier Configurations:-

Common Base	Common Emitter	Common Collector
→ Current Gain (A_I) < 1, and its magnitude decreases with the increase of Load Resistance R_L	→ A_I is high for $R_L < 10K\Omega$.	→ For Low value of R_L ($< 10K\Omega$) A_I is high and almost equal to that of CE
→ Voltage Gain is high for normal values of R_L	→ A_V is high for normal values of R_L.	→ $A_V < 1$ → A_V is high for normal Values of R_L.
→ Input Impedance (R_i). → R_i is medium is lowest		→ R_i is highest of all the three configurations.
→ output Impedance (R_o) → R_o is moderate is highest		→ R_o is lowest of all.

Applications :-

→ Common Base Amplifier :-

(i) used as impedance matching device.

(ii) used as non-inverting amplifier with A_V exceeds unity.

(iii) for driving a high impedance load.

→ Common Emitter Amplifier :-

It alone is capable of providing both A_V and A_I. Further the R_i and R_o are moderately high. Hence it is widely used for Amplification purpose.

→ Common Collector Amplifier :-

(i) widely used as Buffer stage between high impedance source and low impedance load.

(ii) CC amplifier also called as 'Emitter follower'.

Conversion formulae from CE to :-

Common Base	Common Collector
→ $h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	→ $h_{ic} = h_{ie}$
→ $h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	→ $h_{rc} = 1$
→ $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$	→ $h_{fc} = -(1+h_{fe})$
→ $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	→ $h_{oc} = h_{oe}$

Field Effect Transistor (FET)

The FET is a device in which the flow of current through the conducting region is controlled by an Electric field. Hence the name "field Effect Transistor (FET)". As current conduction is only by majority carriers, FET is said to be a unipolar device.

→ Based on the construction, the FET can be classified into two types as
- Junction field Effect Transistor (JFET)
- Metal oxide semiconductor FET (MOSFET)

→ Depending upon the majority carriers, JFET has been classified into two types, namely, (1) N-channel JFET with electrons as majority carriers
(2) P-channel JFET with holes as the majority carriers.

Construction of N-channel JFET:—

It consists of a N-type bar which is made of silicon. ohmic contacts made at the two ends of the bar are called source and drain.

Source (S):— This terminal is connected to the negative pole of the battery. Electrons are majority carriers in the N-type bar enter the bar through this terminal.

Drain (D):— This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

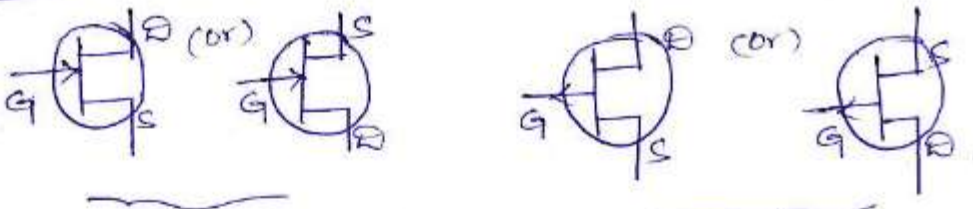
Gate (G):— Heavily doped p-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate 'G'.

channel:- the region of the N-type bar between the depletion region is called the channel.

Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

operation of JFET :—

Symbol :



N-channel JFET P-channel JFET

→ on the two sides of the transition region of a reverse-biased p-n junction there are space charge regions. The current carriers here diffused across the junction, leaving only uncovered positive ions on the n-side and negative ions on the p-side.

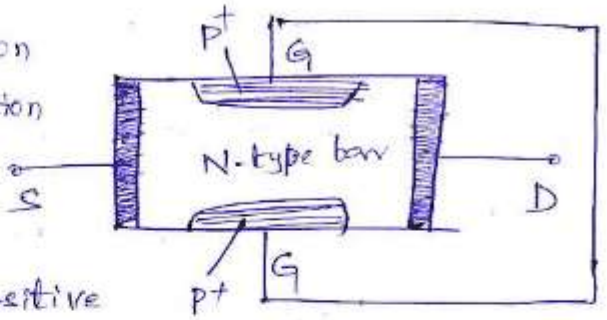


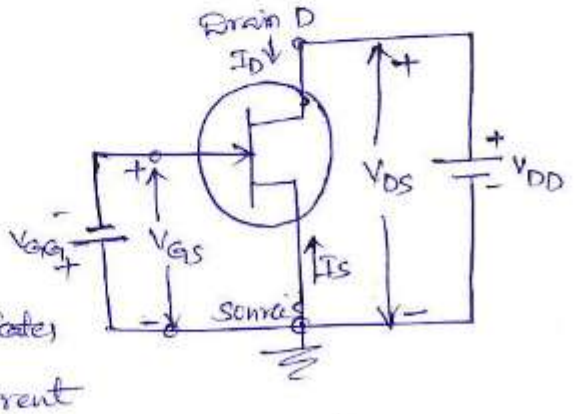
fig: N-channel JFET

The electric lines of field intensity which now originate on the positive ions and terminate on the negative ions.

→ As the reverse bias across the junction increases, the thickness of the region of immobile uncovered charges increases. The conductivity of this region is nominally zero because of the unavailability of current carriers. Hence we see that the effective width of the channel will become progressively decreased with increasing reverse bias.

→ for a fixed drain to source voltage, the drain current will be a function of the reverse biasing voltage across the Gate junction.

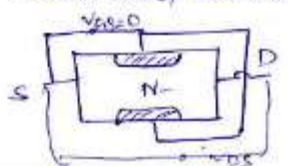
characteristics :—



The circuit Diagram for N-channel JFET shown. The direction of the arrow at the Gate of the junction FET indicates the direction in which gate current would flow if the gate junction were forward biased.

(1) When $V_{GS} = 0$ and $V_{DS} = 0$:—

When no voltage is applied between drain and source and gate and source i.e., Gate, Drain and Source terminals are shorted. So no potential difference between the terminals.



If the potential difference between any two points is zero then the current passes between them is zero. So
Since all the terminals are shorted because of that no charge carriers are moving through the channel so Drain Current is zero when V_{DS} & V_{GS} are zero

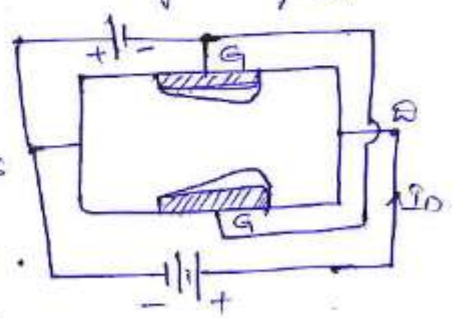
(ii) When $V_{DS}=0$ and V_{GS} is Decreased from zero:

In this case, the PN junctions are reverse biased and hence the thickness of the depletion region increases. Therefore depletion region is more depleted (or penetrate) into the lightly doped region since N-type [i.e, channel] is lightly doped with respect to the p^+ type. so the width of the channel reduces and current passes through the channel reduces with Decrease in V_{GS}.

(iii) When $V_{GS}=0$ and V_{DS} is increased from zero:

Drain is positive with respect to the source with $V_{GS}=0$ and Gate and Source terminals are shorted. so Drain also positive with respect to the Gate. Then there is a potential difference between Source and drain and Gate and drain. Therefore Current passes through the channel.

The potential difference between Gate and Source is zero and there is some potential difference between Drain and Gate. Therefore there is no change in Depletion region width at Source end but there is change in depletion region width at Drain end. Because of potential difference Depletion region penetrates into channel. So the shape is wedge shaped.



The conventional Current I_D flows from Drain to Source. The magnitude of the Current depends upon the following factors:

(1) The number of majority carriers (electrons) available in the channel i.e. the conductivity of the channel.

(2) the length 'L' of the channel.

(3) the cross sectional Area 'A' of the channel.

(4) the magnitude of the applied voltage V_{DS}. Thus the channel acts as a resistor of resistance 'R' is given by $R=\frac{\rho L}{A}$

$$I_D=\frac{V_{DS}}{R}=\frac{A\,V_{DS}}{\rho L}$$

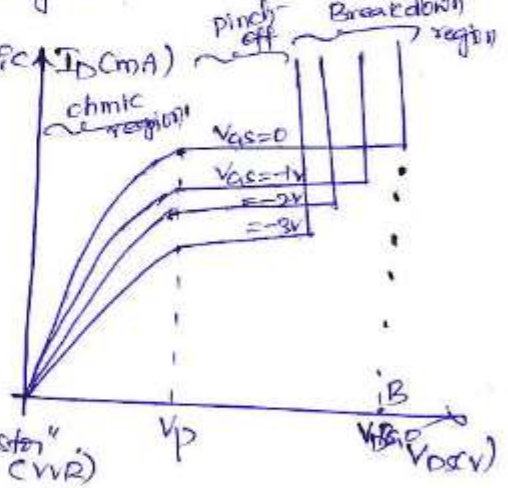
where 'ρ' is the resistivity of the channel.

Because of the resistance of the channel and the applied voltage V_{DS} is a gradual increase of positive potential along the channel from so Drain. Thus the reverse voltage across the PN junctions increases and the thickness of the depletion regions also increases. Therefore, the ch wedge shaped.

→ As V_{DS} is increased, the cross sectional area of the channel will be reduced. At a certain value V_p of V_{DS}, the cross sectional area at Drain end becomes minimum. At this voltage, the channel is said to be pinched off and drain voltage V_p is called the 'pinch off voltage' the region in which current is constant irrespective of voltage is called "pinch off region".

→ As a result of the decreasing cross section of the channel with the increase of V_{DS}, the following results are obtained.

(i) As V_{DS} is increased from zero, I_D increases along OP and the rate of increase of I_D with V_{DS} decreases. The region from $V_{DS}=0$ V to $V_{DS}=V_p$ is called the 'ohmic region".



In the channel ohmic region, the drain to source resistance $\frac{V_{DS}}{I_D}$ is related to the gate voltage V_{GS} in an almost linear manner. This is useful as a 'voltage variable Resistor" (VVR) or 'Voltage Dependent Resistor (VDR)'.

(ii) When $V_{DS}=V_p$, I_D becomes maximum. The length of the pinchoff or saturation region increases. Hence there is no further increase of I_D.

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche Multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain.

The drain at which the breakdown occur is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS}=0$ is shown by the curve OPBC.

(iv) When V_{GS} is negative and V_{DS} is increased :—

When the Gate is maintained at a negative voltage less than the negative Cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS}=0$, but the values of V_p and BV_{DGO} are lower.

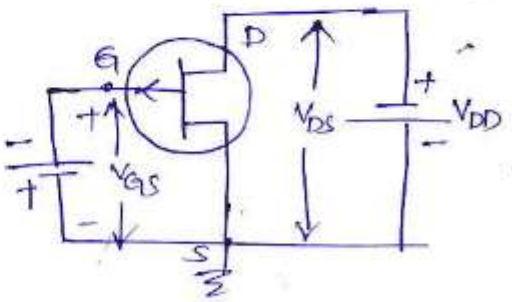
→ from the curves, it is seen that above pinch off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence, a JFET is suitable for use as a voltage amplifier.

→ for voltage $V_{DS}=V_p$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, the ohmic voltage drop along the channel should also be reduced to zero. further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

→ the Drain Current (I_D) is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate. Hence, this device named as "field Effect Transistor".

P-channel JFET :—

In P-channel JFET, the gate is formed due to N-type Semiconductor. In this holes will be the current carriers instead of electrons.



Characteristic parameters of the JFET :—

In a JFET, I_D depends upon the drain voltage V_{DS} and the g voltage V_{GS}. Any one of these variables may be fixed and the relation the other two are determined. These relations are defined as

(1) Mutual Conductance or Transconductance (g_m) :—

It is the slope of the transfer characteristic curves.

It is defined as the ratio of a small change in the drain current to corresponding small change in the gate voltage at a constant dra voltage.

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} \text{ held constant.}$$

(2) Drain Resistance (r_d) :—

It is the reciprocal of the slope of the drain characteristics an defined as the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage.

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, \quad V_{GS} \text{ held constant.}$$

→ The reciprocal of r_d is called the Drain Conductance and is de by g_d or g_{os}.

(3) Amplification factor (μ) :—

It is defined as the ratio of a small change in the drain voltage the corresponding small change in the gate voltage at a constant drain current.

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right) I_D = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, \quad I_D \text{ Constant.}$$

Here negative sign shows that when V_{GS} is increased, V_{DS} must be reduced for I_D to remain constant.

Relationship Among FET Parameters:

As I_D depends on V_{DS} and V_{GS}, the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$ then cossesponding small change in I_D may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus the small change ΔI_D is given by

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

Dividing both sides of the equation by ΔV_{GS},

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$.

$$\therefore 0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

Substituting the values of the partial differential coefficients, we get

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

$$g_m = \frac{\mu}{r_d} \Rightarrow \boxed{\mu = g_m r_d}$$

Therefore the amplification factor (μ) is the product of drain resistance and transconductance (g_m).

Power Dissipation (P_D):—

$$\boxed{P_D = I_D V_{DS}}$$

Pinch off Voltage:—

The Voltage at which, the drain Current I_D tends to level off is called the "pinch off Voltage".

$E_x \rightarrow$ Electric field that appear along x-axis.

→ As V_{DS} increases, E_x and I_D increases whereas the channel width $b(x)$ narrows. Therefore the $J_D = I_D / 2b(x)W$ increases.

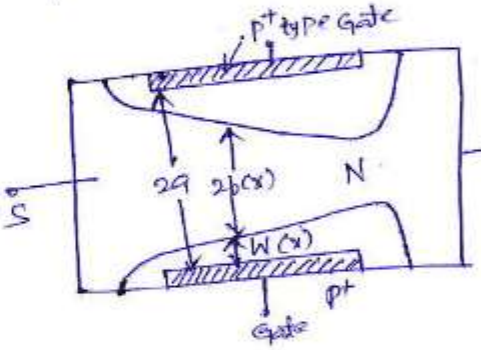
$$\because I_D = A q N_D \mu_n E_x$$

Since $J = nq\mu E = N_D \mu_n q E$ [Since $n \cong N_D$, $\mu = \mu_n$; & $J = \sigma E$, $J = I/A$]

$$\therefore I = A * J$$

where $A = 2b(x)W$

considering 'b' along x-axis. Since 'b' depends upon the voltage V_{gs}. $b(x)$ is the width at any point 'x'.



$$I_D = 2b(x) W q N_D \mu_n E_x$$

$$\because E_x = \frac{V_{DS}}{L}$$

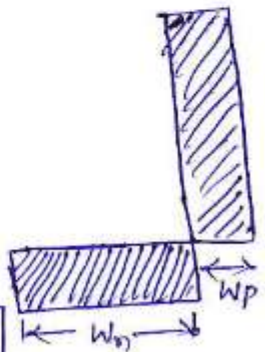
$$\therefore \boxed{I_D = 2b(x) W q N_D \mu_n \frac{V_{DS}}{L}}$$

As V_{DS} increases, E_x increases but mobility reduces. so 'b' almos Constant. Therefore I_D remains constant in the pinch off region.

Expression for pinch off Voltage:—

Net change in an alloy junction must be same, Semi Conductor remains neutral.

If $N_A >> N_D$, $W_p << W_n$.



from poisson's equation.

$$\frac{d^2V}{dx^2} = \frac{qN_D}{\epsilon}$$

$\rho \rightarrow$ charge density

$\frac{d^2V}{dx^2} = \rho/\epsilon$.

where $\rho = qN_D$

We can neglect W_p and assume that the entire barrier potential V_B appears across the increased donor ion

$$\frac{dV}{dx} = \frac{qN_D}{\epsilon} x$$

$$V = \frac{qN_D}{\epsilon}\frac{x^2}{2}$$

At the Boundary condition, $x = w_n$ where $w_n \rightarrow$ Depletion region width

$$V = \frac{qN_D}{2\epsilon} w_n^2 \Rightarrow w_n = \left\{\frac{2\epsilon V}{qN_D}\right\}^{1/2}$$

This is the expression for the Penetration of depletion region into the channel. The general expression for the space charge width,

$$w_n(x) = w_n.$$

$$W(x) = \left[\frac{2\epsilon}{qN_D}\{V_0 - V(x)\}\right]^{1/2} \quad \text{where } V = V_0 - V(x)$$

$V_0 \rightarrow$ Contact potential at x.

$V(x) \rightarrow$ not uniform throughout the channel.

The potential is higher near the drain and decreases towards the source.

$\therefore V = V_0 - V(x)$

$$a - b(x) = W(x) = \left\{\frac{2\epsilon}{qN_D}(V_0 - V(x))\right\}^{1/2}$$

$a - b(x) \rightarrow$ penetration $W(x)$ of depletion region into channel at a point x along the channel from one side of gate region.

$$W = \left\{\frac{2\epsilon}{qN_D} \cdot V_p\right\}^{1/2}$$

$V_{GS} = V_0 - V(x)$ in the space charge width equation, we get

$$a - b(x) = \left\{\frac{2\epsilon}{qN_D} \cdot V_{GS}\right\}^{1/2}$$

upon solving we get,

$$a - b(x) = \left[\frac{a^2}{V_p} \cdot V_{GS}\right]^{1/2}$$

further simplifying, $\frac{a - b(x)}{a} = \left(\frac{V_{GS}}{V_p}\right)^{1/2}$

Therefore, $\left[1 - \frac{b(x)}{a}\right]^2 = \frac{V_{GS}}{V_p}$

Hence Gate Source voltage is,

$$\boxed{V_{GS} = \left[1 - \frac{b(x)}{a}\right]^2 V_p}$$

JFET Small Signal Model:

From the drain and transfer characteristics of the FET, the drain current of an FET is a function of Drain to Source voltage (V_{DS}) and gate to Source voltage (V_{GS}).

Assuming varying currents and voltages for an FET,

$$i_D = f(V_{GS}, V_{DS})$$

If both Gate and drain voltages are varied, the change in drain current is given approximately by first two terms in the Taylors series expansion,

$$\Delta i_D = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS} + \left(\frac{\partial i_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS}$$

in Small signal notation as for BJT,

$$\Delta i_D = i_d, \quad \Delta V_{GS} = V_{gs} \text{ and } \Delta V_{DS} = V_{ds}.$$

$$\therefore \quad i_d = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} V_{gs} + \left(\frac{\partial i_D}{\partial V_{DS}}\right)_{V_{GS}} V_{ds}$$

$$\boxed{i_d = g_m V_{gs} + \frac{1}{R} V_{ds}}$$

where Mutual Conductance or Transconductance of the FET is defined as,

$$\boxed{g_m = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} = \left(\frac{\Delta i_D}{\Delta V_{GS}}\right)_{V_{DS}} = \left(\frac{i_d}{V_{gs}}\right)_{V_{DS}}}$$

and drain (or o/p) resistance of the FET is defined as

$$\boxed{r_d = \left(\frac{\partial V_{DS}}{\partial i_D}\right)_{V_{GS}} = \left(\frac{\Delta V_{DS}}{\Delta i_D}\right)_{V_{GS}} = \left(\frac{V_{ds}}{i_d}\right)_{V_{GS}}}$$

The reciprocal of r_d is the drain Conductance g_d.

An amplification factor μ for an FET may be defined as

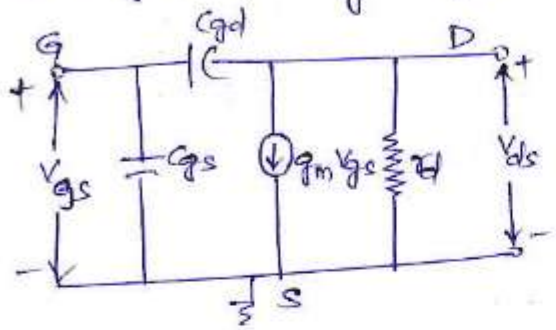
$$\mu = \left(\frac{-\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = \left(\frac{-\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} = g_m r_d.$$

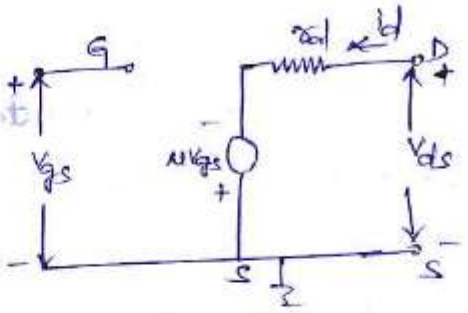
The Small signal models for the Common Source FET can be used for analysing three basic FET amplifier configurations. They are

(i) Common Source (CS) (ii) Common Drain (CD) (iii) Common Gate (CG)

Common Source amplifier which provides good voltage amplification is most frequently used.

→ Common Drain amplifier with high i/p impedance and near unity voltage gain is used as a buffer amplifier and the CG amplifier is used as high frequency amplifier.





Prove that $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$.

(VU)

for Common Base.

$$h_{fb} = \frac{I_c}{I_e} = \frac{I_c}{I_b} * \frac{I_b}{I_e}$$

$$= \frac{h_{fe}}{(I_e/I_b)} \quad (\because h_{fe} = I_c/I_b)$$

$$= \frac{h_{fe}}{-(I_c+I_b)/I_b} = \frac{-h_{fe}}{1+I_c/I_b}$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$$

Hence proved.

Expression for saturation Drain Current:

* for the transfer characteristics, V_{DS} is maintained constant at a suitable value greater than the pinch off voltage V_p. the gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. the transfer char's are shown.

The shape of the transfer characteristics is very nearly a parabola. It is found that the char'n is approx represented by the parabola.

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

I_{DS} → Saturation Drain Current

I_{DSS} → Value of I_{DS} when $V_{GS}=0$

By differentiating,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} * 2\left[1 - \frac{V_{GS}}{V_p}\right]\left[-\frac{1}{V_p}\right]$$

$$\therefore g_m = \frac{\delta I_{DS}}{\delta V_{GS}}, \quad V_{DS} \text{ is constant.}$$

$$\therefore \boxed{g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]}$$

* we have $\left(1 - \frac{V_{GS}}{V_p}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$

$$\therefore g_m = \frac{-2I_{DSS}}{V_p} * \sqrt{\frac{I_{DS}}{I_{DSS}}} = \frac{-2\sqrt{I_{DSS} \cdot I_{DS}}}{V_p}$$

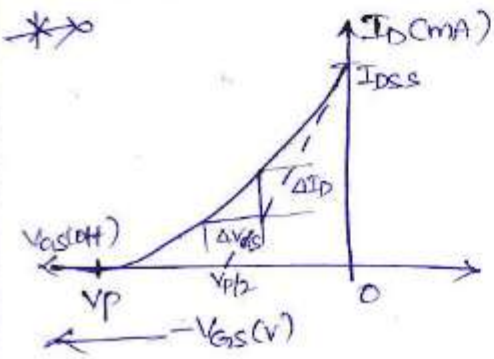
Suppose if $g_m = g_{m0}$ when $V_{GS}=0$ then

$$g_{m0} = \frac{-2I_{DSS}}{V_p}$$ therefore, $\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)}$

Slope of the Transfer characteristics at I_{DSS} is

$$\boxed{g_m = \frac{2\sqrt{I_{DS} I_{DSS}}}{V_p}}$$

**



Transfer characteristics of JFET

MOSFET [Metal Oxide Semi-Conductor field Effect Transistor]:-

MOSFET is an Integrated circuit or Semi conductor chip.

→ MOSFET is fabricated by VLSI by using planar technology.

→ MOSFET is a symmetrical device.

→ It has the larger input resistance due to the SiO_2 layer.

→ Generally FET's are operated in two modes. They are
(1) Enhancement mode (2) Depletion Mode

→ In Enhancement mode, channel is creating after applying field.
In Depletion mode, channel is pse-existing.

→ MOSFET's are two types. They are (1) p-channel MOSFET
(2) N-channel MOSFET

P-channel MOSFET is operated in Enhancement mode only but the N-channel MOSFET is operated in Enhancement and Depletion modes. So N-MOSFET sometimes called "Dual MOSFET".

→ NMOS is faster than PMOS, because electron mobility is greater than hole mobility.

→ To get equal performance between NMOS & PMOS, PMOS requires twice the area required for NMOS.

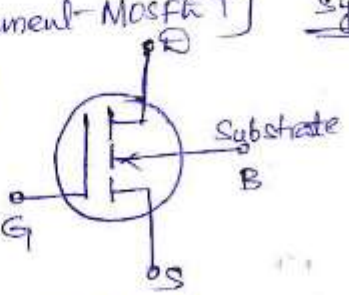
→ PMOS is bulky and cheap.

→ PMOS is easier to fabricate than NMOS.

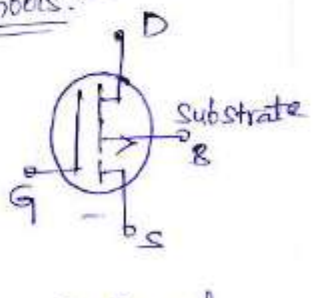
Construction:- [N-channel Enhancement-MOSFET]

As there is no continuous channel in an Enhancement MOSFET, this condition is represented by the broken line in the symbols.

Symbols:-



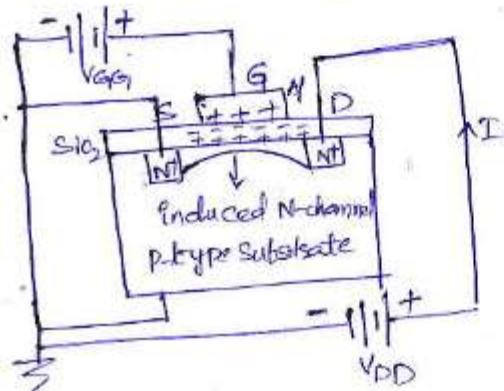
N-channel



P-channel

Enhancement-MOSFETS

→



→ Two highly doped N^+ regions are diffused in a lightly doped p-type silicon substrate. one N^+ region is called the "Source" and the other one is called the "Drain". They are separated by 1mm.

A thin layer of insulating SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer allowing contact with the source & drain. Then a thin layer of metal (Al) is overlaid on the oxide, covering the entire channel region. Simultaneously, metal contacts made to the drain and source. The contact to the metal over the channel area is the Gate terminal.

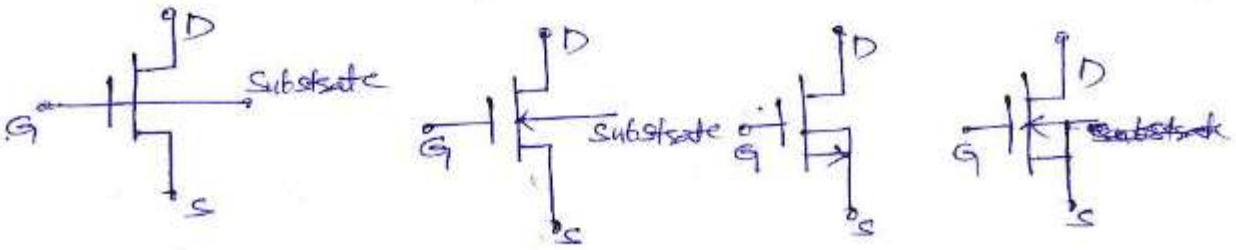
Because of SiO_2 layer over the substrate, MOSFET has high input impedance. The metal area of the Gate in conjuction with the insulating dielectric oxide layer and the semiconductor channel forms a parallel plate capacitor. Because of the insulating layer of SiO_2 on the substrate, the device name is called 'Insulated Gate FET'.

Operation of N-channel Enhancement MOSFET :—

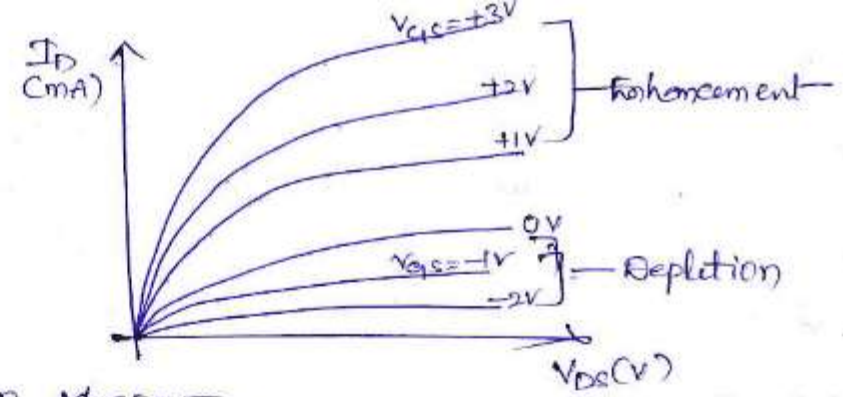
If the substrate is grounded and a positive voltage is applied at the Gate, the positive charge on Gate induces equal negative charge on the substrate side between the source and drain regions. The direction of E-field perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the p-type substrate forms an inversion layer.

As the positive voltage on the Gate increases, the induced negative charge in the semiconductor increases. Hence the conductivity increases. and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate voltage.

Symbols for N-channel Enhancement MOSFET(or) E-only MOSFET :



V-I characteristics:



N-channel Depletion MOSFET:—

The construction of an N-channel depletion MOSFET shown in figure. where an N-channel is diffused between the source and drain.

With $V_{GS}=0$ and the Drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the N-channel from source to Drain. Therefore, the conventional current I_D flows through the channel Drain to source.

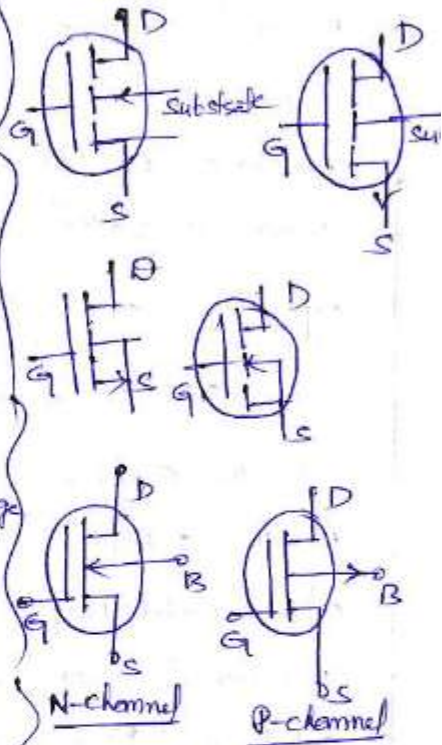
→ If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel. The shape of depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped.

→ when V_{DS} increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the "pinch off voltage". The drain current I_D almost gets saturated beyond pinch off voltage.

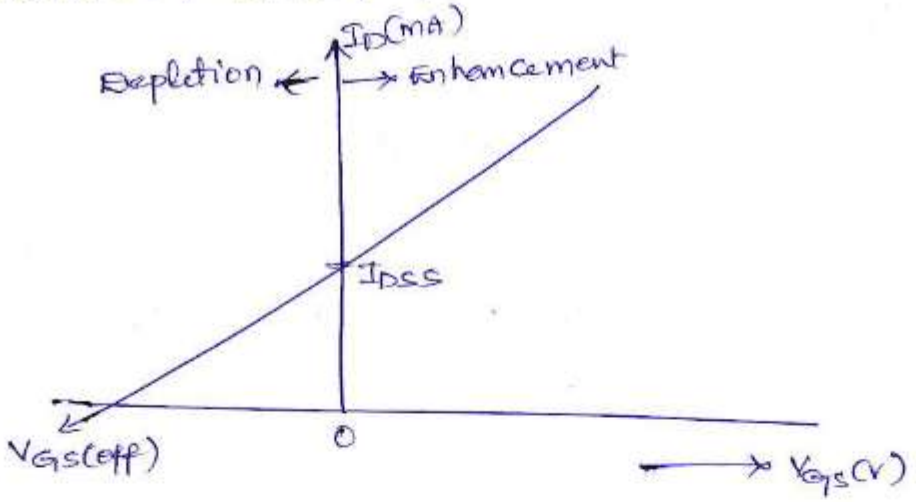
→ Since the current in an FET is due to majority carriers, the induced positive charges make the channel less conductive and I_D drops as V_{GS} is made negative.

→ The depletion MOSFET can also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the N-type channel. Hence, the conductivity of the channel increases and I_D increases.

Symbols:



The curve of I_D versus V_{GS} for constant V_{DS} is called the "Transfer characteristics of MOSFET".



Comparison between Depletion MOSFET and E-only MOSFET:

Depletion MOSFET	Enhancement MOSFET
→ There is pre-existing channel.	→ There is no pre-existing channel and channel has to be created by applying proper gate to source voltage.
→ channel is diffused channel.	→ channel is induced channel.
→ Suitable to operate both in the depletion mode and Enhancement mode	→ Suitable to operate only in the Enhancement mode.
→ Comparatively larger threshold voltage	→ Comparatively V_T is very small.
→ There is no channel length Modulation.	→ channel length modulation exists.
→ when $V_{GS}=0$, I_D flows and is equal to I_{DSS}.	→ If V_{GS} kept zero, there is no channel hence I_D is zero.

Channel length Modulation:—

When V_{DS} is applied the length of the channel reduces. The process where the length of the channel changes by varying V_{DS} is called "channel Length Modulation".

Equation for NMOS:—

Over drive Voltage V_{ov}:—

It is the voltage where the device enters into saturation.

$$V_{ov} = V_{DS(sat)}, \quad V_{ov} = (V_{GS} - V_T)$$

→ Triode region indicates ohmic region or linear region.

→ Saturation region also called "Pentode Region". $V_{DS(sat)} = (V_{GS} - V_T)$.

Operation in the Triode Region:—

If $V_{DS} < V_{DS(sat)}$

i.e., $V_{DS} < (V_{GS} - V_T)$ or $V_{DS} < V_{GS}$

$$i_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Let $\mu_n C_{ox} = k_n$ → process transconductor parameter in $A m/V^2$.

$$i_d = k_n \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Let $k_n \frac{W}{L} = K$.

Let in Triode Region V_{ds} is small then V_{ds}^2 is very small.

$$\therefore \boxed{i_d = K [V_{gs} - V_T] V_{ds}}$$

The above equation is of first order and this indicates the triode Region. The curve is always a straight line.

→ The drain to source resistance of FET is

$$r_{ds} = \frac{V_{ds}}{i_d} = \frac{V_{ds}}{K[V_{gs} - V_T] V_{ds}} \approx \frac{1}{K[V_{gs} - V_T]} \Omega$$

$$r_{ds} = \frac{1}{K V_{ov}} \Omega$$

$$\therefore \boxed{r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} [V_{gs} - V_T]} \Omega}$$

The above equation indicates that in the triode Region, FET can work as a voltage variable Resistor by varying gate to source voltage.

→ Transconductance of FET in the triode region is given by

$$g_m = \frac{\partial i_d}{\partial V_{gs}} \mho$$

$$g_m = K V_{ds} \quad \because i_d = (V_{gs} - V_T) V_{ds}$$

$$\therefore \boxed{g_m = \mu_n C_{ox} \frac{W}{L} V_{ds}} \mho$$

Operation in the Saturation Region (or) Pentode Region :—

Condition: $V_{DS} \geq V_{DS(sat)}$

$V_{DS} \geq [V_{GS} - V_T]$ i.e., $\boxed{V_{DS} > V_{GS}}$

$$i_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2$$

The second order equation and this indicates, in the saturation region i_d increases as a parabolic variation with V_{GS}.

$$i_d = \frac{1}{2} k_n \frac{W}{L} [V_{GS} - V_T]^2 \quad \text{Let } K = \frac{1}{2} k_n \frac{W}{L}$$

$$\therefore \boxed{i_d = K [V_{GS} - V_T]^2}$$

In the saturation region, the transconductance g_m is

$$g_m = \frac{\partial i_d}{\partial V_{GS}} = 2K [V_{GS} - V_T] \text{ V}$$

$$g_m = 2 * \tfrac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]$$

$$\therefore \boxed{g_m = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]} \text{ V}$$

Where C_{ox} → oxide capacitance per unit area

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \text{ F/m}^2$$

ϵ_{ox} → permittivity

$\epsilon_{ox} = \epsilon_0 \epsilon_r$

$\epsilon_r = 3.9$ for SiO_2

$\epsilon_0 = 8.854 * 10^{-12}$ F/m

$\boxed{C_{gate} = C_{ox} \cdot W \cdot L}$ farads

FET - Amplifiers (Field Effect Transistor Amplifiers) :—

→ Field Effect Amplifiers (FET) provide an excellent voltage gain with the added feature of high input impedance. They have low power consumption & with a good frequency range and minimal size and weight. The noise output level is low. This feature makes them very useful in the amplifier circuits.

→ Because of the high input impedance characteristic of FETs, the ac equivalent model is simpler than that employed for BJTs.

→ Various FET amplifiers are

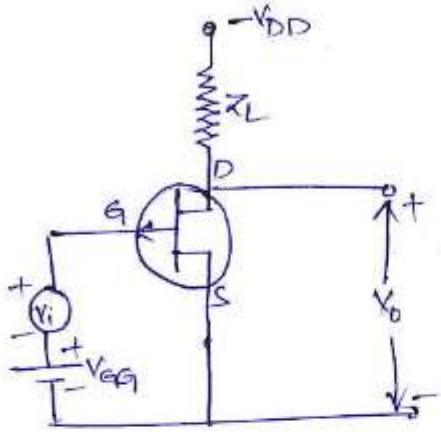
→ Common Source amplifier → Common Drain amplifier → Common Gate amplifier

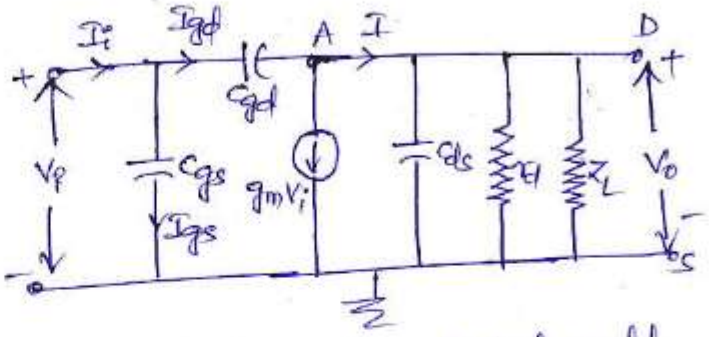
→ The Common Source configuration is the most popular one, providing an inverted and amplified signal.

→ Common Drain (Source follower) circuits providing unity gain with no inversion.

→ Common Gate circuits providing gain with no inversion.

Common Source Amplifier:





Small signal equivalent model

Voltage Gain (A_V):

If the FET is replaced by its small signal high frequency model, Gain can be obtained as follows.

The parallel combination of Z_L, C_{ds} and r_d can be replaced by an impedance Z between the terminals D & S where Z is given by

$$Z = \frac{1}{Y_L + Y_{ds} + g_d} \quad \text{where} \quad Y_L = \frac{1}{Z_L}$$

$Y_{ds} = j\omega C_{ds}$ = Admittance corresponds to C_{ds}

$$g_d = \frac{1}{r_d}$$

The voltage across capacitor C_{gd} is $V_i - V_o$. Thus the current I_{gd} passing through the gate drain capacitor is

$$I_{gd} = Y_{gd}(V_i - V_o)$$

By applying KCL at node A, the current I passing through Z is given by $I = -g_m V_i + I_{gd} = (-g_m + Y_{gd})V_i - Y_{gd} V_o$

∴ The o/p voltage $V_o = IZ$. We get

$$V_o = \frac{(-g_m + Y_{gd})V_i - Y_{gd} V_o}{Y_L + Y_{ds} + g_d}$$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}}$$

At low frequencies, the FET capacitances can be neglected. Under this conditions,

$Y_{ds} = Y_{gd} = 0$ & A_V reduces to

$$A_V = \frac{-g_m}{Y_L + g_d} = \frac{-g_m Z_L}{1 + g_d Z_L} = -g_m Z_L'$$

where $Z_L' = r_d // Z_L$

Input Admittance:—

Current through C_{gs} is $I_{gs} = Y_{gs} V_i$. Thus the total input current I_i' can be written as

$$I_i' = I_{gs} + I_{gd} = Y_{gs} V_i + Y_{gd}(V_i - V_o) \quad \text{where } Y_{gs} = j\omega C_{gs}$$

Since the input admittance of the circuit is

$$Y_i = \frac{I_i'}{V_i}, \text{ we can write}$$

$$Y_i = Y_{gs} + Y_{gd}(1 - A_V)$$

where $A_V = \frac{V_o}{V_i}$ → Gain of the Amplifier

This expression indicates that for a FET to possessive negligible input admittance over a wide range of frequencies, C_{gs} and C_{gd} must be negligible.

Input Capacitance:—

$$\because A_V = -g_m R_d' \quad \text{where } R_d' = R_d // r_d \qquad \left[\because \text{let } Z_L' = R_d' \;\; Z_L = r_d\right]$$

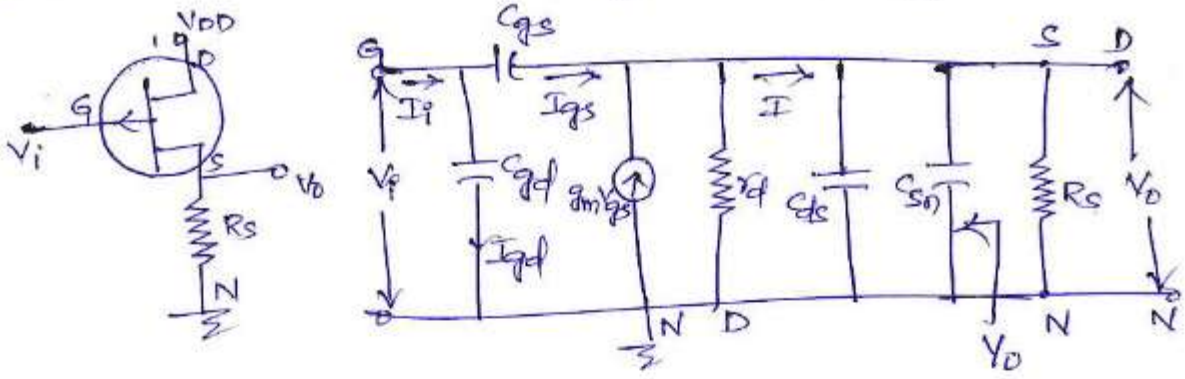
$$\frac{Y_i'}{j\omega} = C_1 = C_{gs} + (1 + g_m R_d') C_{gd}.$$

Output Resistance:—

$$R_o = R_d // r_d.$$

It is valid at low frequencies, where the effect of the capacitor is negligible and with resistive load. $Z_L = R_d$.

Common Drain Amplifier :— [Source-Follower]



In this additional capacitance C_{sn} is added in the equivalent circuit which represents the capacitor from source to ground.

Voltage Gain (A_V) :—

Internal Current Generator output is proportional to V_{gs} where $V_{gs} = V_i - V_o$ is the voltage across the gate-source. We can easily write

$$z = \frac{1}{g_d + j\omega(C_{ds} + C_{sn}) + 1/R_s}$$

$$I_{gs} = j\omega C_{gs}(V_i - V_o) \quad \text{and} \quad I = I_{gs} + g_m(V_i - V_o)$$

where $z \rightarrow$ Resultant Impedance of the parallel combination of the impedances corresponding to r_d, C_{ds}, C_{sn} and R_s, I_{gs} is the current passing through C_{gs}.

$I \rightarrow$ Current passing through z.

from $V_o = Iz$, we can write

$$V_o = \frac{(g_m + j\omega C_{gs})(V_i - V_o)}{g_d + j\omega(C_{ds} + C_{sn}) + 1/R_s}$$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

Amplification is positive and has a value less than unity.

If $g_m R_s >> 1$, then $A_V = \frac{g_m}{(g_m + g_d)} = \frac{\mu}{\mu + 1}$ //

Input Admittance (Y_i) :—

It offers the important advantage of lower input capacitance than CS amplifier.

Since $I_{gd} = j\omega C_{gd} V_i$

$$I_{gs} = j\omega C_{gs}(V_i - V_o)$$

The input current I_i is given by

$$I_i = I_{gd} + I_{gs} = (j\omega C_{gd} + j\omega C_{gs}(1-A_V))V_i$$

then the input admittance, Y_i is

$$\boxed{Y_i = \frac{I_i}{V_i} = j\omega C_{gd} + j\omega C_{gs}(1-A_V)}$$

Output Admittance:—

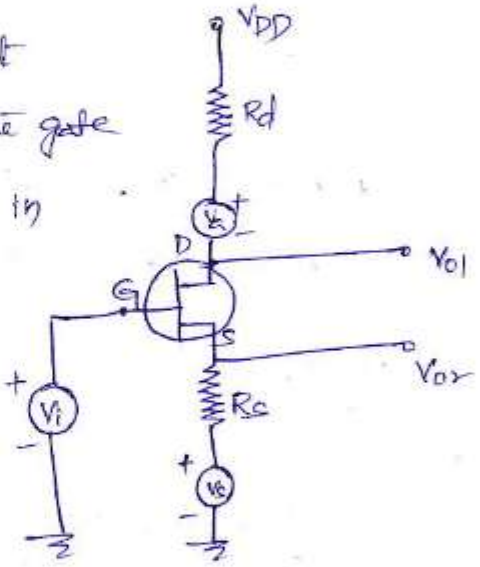
$$Y_o = g_m + g_d + j\omega C_T$$

$$R_o = \frac{1}{g_m + g_d} \simeq \frac{1}{g_m}$$

FET offers high input impedance and low o/p impedance.

A Generalized FET Amplifier:—

The circuit contains three independent signal source, V_i in series with the gate V_s in series with the source and V_d in series with the drain.

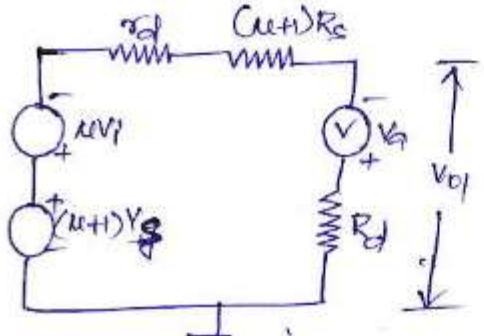


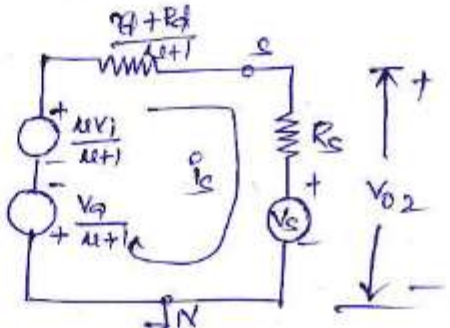
For the Common source amplifier, $V_s = V_d = 0$ and the output is V_{o1} taken at the drain.

for the common gate circuit, $V_i = V_d = 0$, the signal is V_s. V_s with a source resistance R_s and the output is V_{o1}.

for the source-follower [common Drain], $R_d = 0$, $V_d = V_s = 0$. The signal voltage is V_i and the output is V_{o2} taken at the source.

From the Thevenin's equivalent circuit of the above figure, from Drain to ground and from Source to ground.





From the first circuit, we conclude that if we looking into the drain of the FET, we see an equivalent circuit consisting of two generators in series, one of $-\mu$ times the gate signal voltage V_i and the second $(\mu+1)$ times the source signal voltage V_s and the resistance

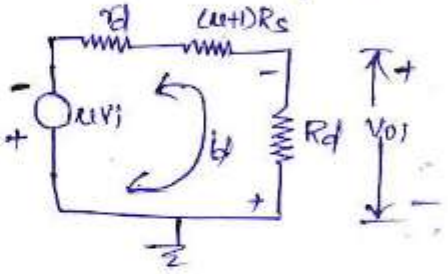
$r_d + (\mu+1) R_s$.

→ The voltage V_s and the resistance in the source lead are both multiplied by the same factor, $\mu+1$.

Common Source amplifier with an unbypassed Source Resistance:-

From the figure (1), $V_s = V_a = 0$, we obtain the voltage gain

$$A_V = \frac{V_{o1}}{V_i}$$



By applying KVL,

$$+\mu V_i - i_d r_d - (\mu+1) R_s i_d - i_d R_d = 0$$

$$\mu V_i = i_d [r_d + (\mu+1) R_s + R_d] \Rightarrow V_i = \frac{i_d}{\mu} [r_d + (\mu+1) R_s + R_d]$$

$$V_{o1} = -i_d R_d$$

$$\therefore A_V = \frac{-i_d R_d}{\frac{i_d}{\mu}[r_d + (\mu+1) R_s + R_d]} \Rightarrow \boxed{A_V = \frac{-R_d * \mu}{r_d + (\mu+1) R_s + R_d}}$$

$\because \mu = g_m * r_d$

$$\therefore A_V = \frac{-g_m r_d R_d}{r_d \left[1 + \frac{(\mu+1)}{r_d} R_s + \frac{R_d}{r_d}\right]} = \frac{-g_m R_d}{1 + (g_m r_d + 1)\frac{R_s}{r_d} + \frac{R_d}{r_d}}$$

$$\boxed{A_V = \frac{-g_m R_d}{1 + g_m R_s + (R_s + R_d) g_d}} \quad \text{where } g_d = 1/r_d$$

where the minus sign indicates a 180° phase shift between input and output.

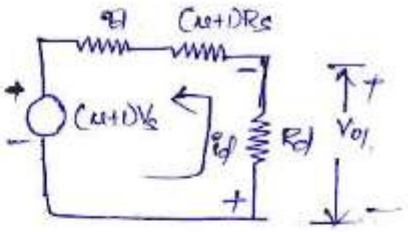
The resistance R_o, looking into the drain, is increased by $(\mu+1)R_s$ from its value r_d for $R_s = 0$. considering R_D, the net output resistance R_o is

$$\boxed{R_o = (r_d + (\mu+1) R_s) \,//\, R_D}$$

The additional R_s reduces the voltage gain and increases the output impedance

The Common Gate Amplifier :—

from figure ①, with $V_i = V_a = 0$, we obtain the voltage gain $A_V = V_{o1}/V_s$.



By KVL,

$$-(u+1)V_s - i_d r_d - (u+1)R_s \cdot i_d - i_d R_d = 0$$

$$(u+1)V_s = -i_d\left[r_d + (u+1)R_s + R_d\right]$$

$$V_s = \frac{-i_d}{(u+1)}\left[r_d + (u+1)R_s + R_d\right]$$

and $$V_{o1} = -i_d R_D$$

$$\therefore A_V = \frac{V_{o1}}{V_s} = \frac{i_d R_d}{\frac{i_d}{(u+1)}\left[r_d + (u+1)R_s + R_d\right]} = \frac{(u+1)R_d}{r_d + (u+1)R_s + R_d}$$

Since $u = g_m r_d$

$$\therefore A_V = \frac{(g_m r_d + 1)R_d}{r_d + (u+1)R_s + R_d} = \frac{r_d\left[g_m + 1/r_d\right]R_d}{r_d\left[1 + (u+1)\frac{R_s}{r_d} + \frac{R_d}{r_d}\right]} = \frac{(g_m + g_d)R_d}{1 + \frac{g_m r_d R_s}{r_d} + \frac{R_s}{r_d} + \frac{R_d}{r_d}}$$

$$\boxed{A_V = \frac{(g_m + g_d)R_d}{1 + g_m R_s + g_d\left[R_s + R_d\right]}} \qquad \text{where } g_d = 1/r_d$$

Since A_V is a positive number. There is no phase shift between input and output.

Since $g_m \gg g_d$, the magnitude of the amplification is approximately the same as for the CS amplifier with $R_s \neq 0$.

The output resistance R_o' is given by

$$R_o' = \left[r_d + (u+1)R_s\right] /\!/ R_d .$$

unless R_s is quite small. R_o' will be much larger than $r_d /\!/ R_d$. The input impedance R_i' between source and ground is obtained by

$$R_i' = \left(\frac{r_d + R_d}{u+1}\right) /\!/ R_s$$

The Common Gate amplifier has low input resistance and high output resistance.

The output from the source:

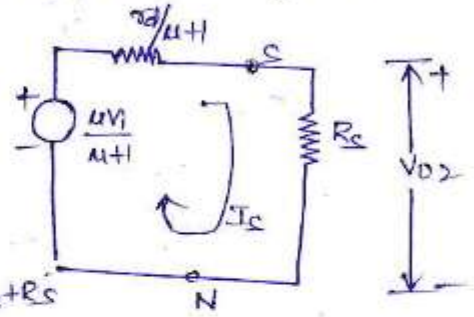
If we looking into the source of the FET, we see an equivalent circuit consisting of two generators in series, one of value $\frac{\mu}{\mu+1}$ times the gate signal voltage V_i and the second $\frac{1}{\mu+1}$ times the drain signal voltage V_0 and a resistand $(R_d + R_d)/(\mu+1)$.

The voltage V_0 and the resistance in the drain circuit are both divided by the same factor $(\mu+1)$.

Common Drain Amplifier: ——— [Source follower]

from Eqn ⑤, with $V_s = V_a = 0$ and $R_d = 0$. Then the voltage Gain (A_V) is

$$A_V = \frac{V_{02}}{V_i} = \frac{\mu R_s/(\mu+1)}{[r_d/(\mu+1)] + R_s}$$



Since $\mu = g_m r_d$,

$$A_V = \frac{g_m r_d \cdot R_s}{(g_m r_d + 1)} \cdot \frac{(g_m r_d + 1)}{r_d + R_s(\mu+1)} = \frac{g_m r_d R_s}{r_d + g_m r_d R_s + R_s}$$

$$A_V = \frac{r_d(g_m R_s)}{r_d[1 + g_m R_s + R_s]} = \frac{g_m R_s}{1 + g_m R_s + g_d R_s} = \frac{g_m R_s}{1 + (g_m + g_d) R_s}$$

The output impedance R_0 of the source follower at low frequencies (with $R_d = 0$ and with R_s considered external to the amplifier), is

$$R_0 = \frac{r_d}{\mu+1} = \frac{1}{g_m + g_d}$$

The o/p impedance R_0', taking R_s into account is $R_0' = R_0 // R_s$.

Biasing FET:

for the proper functioning of a linear FET amplifier. It is necessary to maintain the operating point 'Q' stable in the central portion of the pinch off region.

The Q-point should be independent of device parameter variations and temperature variation. This can be achieved by suitably selecting the V_{GS} and I_D. which is referred to as "Biasing".

Fixing the Q-point :—

The Q-point, the quiscent point or operating point for a self biased JFET is established by determining the value of drain Current I_D for a desired value of Gate to Source voltage, V_{GS} or viceversa.

→ If the data sheet of JFET includes a transfer characteristics Curve, then the Q-point may be determined by using the procedure given below.

(i) Select a convenient value of drain Current whose value is generally taken half of the maximum possible value of drain Current I_{DSS} then find the voltage drop across Source resistor R_S, by

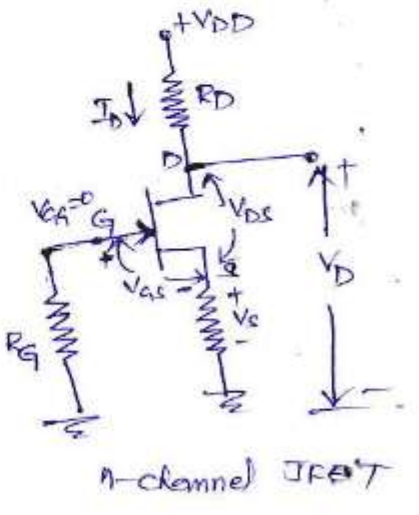
$$V_S = I_D R_S$$

and the gate to Source voltage from the equation $V_{GS} = -V_S$.

(ii) Plot the assumed value of drain Current I_D and the corresponding gate to Source voltage V_{GS} on the transfer characteristic Curve.

(iii) Draw a line through the plotted point and the origin. The point of intersection of the line and the curves gives the desired Q-point then read the coordinates of Q-point.

Self Biasing of FET:



From the circuit,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D [R_D + R_S]$$

$$V_D = V_{DD} - I_D R_D$$

$$V_{GG} - V_{GS} - V_S = 0 \Rightarrow V_{GS} = V_{GG} - V_S$$

$$\therefore V_{GS} = -I_D R_S$$

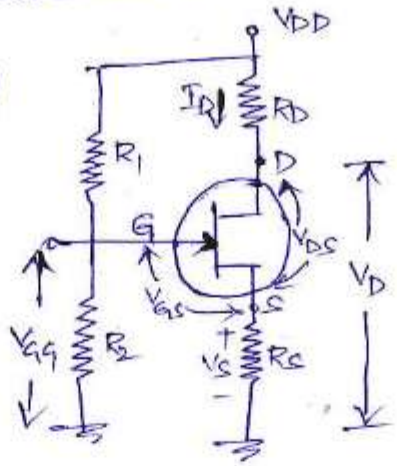
When the drain voltage V_{DD} is applied, a drain Current I_D flows even in the absence of gate voltage V_G. The voltage drop across the resistor R_S produced by the drain Current is given by $V_S = I_D R_S$. This voltage drop reduces the gate to Source reverse voltage required for FET operation. This feedback resistor R_S prevents any variation in

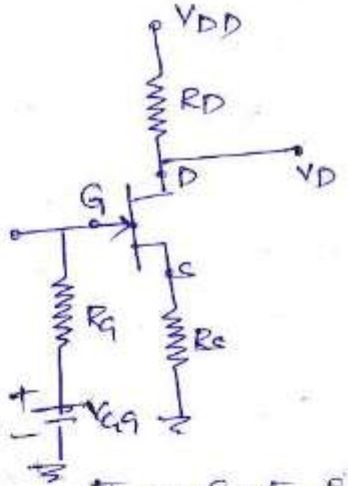
Voltage Divider Biasing of FET:-

Resistors R_1 & R_2 connected on the gate side forms a voltage divider. The gate voltage

$$V_{GG} = \left(\frac{R_2}{R_1+R_2}\right)V_{DD}$$

$$R_G = \frac{R_1 R_2}{R_1+R_2}$$





Thevenin equivalent circuit

The bias line satisfies the equation. $V_{GS} = V_{GG} - I_D R_S$

The Drain to gate voltage $V_D = V_{DD} - I_D R_D$.

→ If V_{GG} is very large as compared to gate to source voltage V_{GS}, the drain current is approximately constant.

→ In practice, the voltage divider bias is less effective with JFET than BJT.

→ In a JFET, the V_{GS} can vary several volts from one JFET to another.

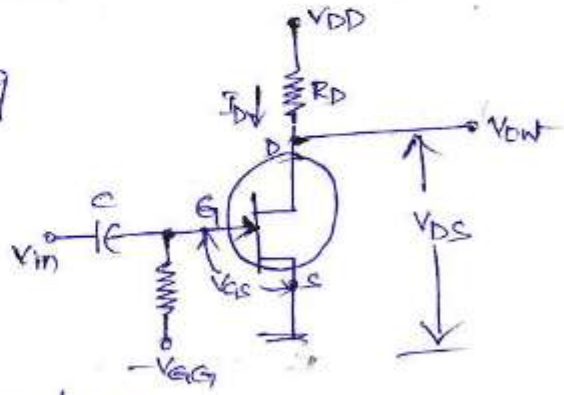
$$V_{DD} - I_D R_D - V_{DS} - V_S = 0$$

$$V_{DD} - I_D R_D - V_D = 0 \Rightarrow V_D = V_{DD} - I_D R_D$$

Fixed Bias:-

The FET device needs DC bias for setting the gate to source voltage V_{GS} to give desired drain current I_D.

→ For a JFET, the drain current is limited by I_{DSS}.



→ Since the FET has a high input impedance, it does not allow the gate current to flow and the dc voltage of the gate set by a voltage divider or a fixed battery is not affected or loaded by the FET.

→ The fixed bias circuit for an N-channel JFET shown in figure is obtained by using a supply V_{GG}. This supply ensure that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal i.e. $I_G = 0$.

The V_{GG} supply provides a voltage V_{GS} to bias the N-channel JFET. But no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any AC signal applied through capacitor C to develop across R_G. while any AC signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ which is equal to zero volt.

The Gate to Source voltage V_{GS} is

$$V_{GS} = V_G - V_S = -V_{GG} - 0 = -V_{GG}$$

The Drain to Source Current I_D is then fixed by the Gate Source voltage. This Current will cause a voltage drop across the drain resistor R_D and is given by

$$V_{DD} = I_D R_D + V_{DS}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

FET as Voltage Variable Resistor (VVR):—

FET is operated in the Constant Current portion of it's output characteristics for the linear applications.

In the region before pinch off, where V_{DS} is small the drain to Source resistance 'r_d' can be controlled by the bias voltage V_{GS} i.e. As the V_{GS} value changes Id value changes then drain resistance also changes with respect to V_{GS}.

As V_{GS} increases [(or) decreasing negative V_{GS}] drain Current increases then r_d value reduces. So hose r_d can be Controlled by V_{GS}.

So resistance of FET changes therefore the FET is useful as a "voltage variable Resister (VVR)" or "voltage Dependent Resister (V.D.R)".

Comparison of JFET and BJT:

JFET	BJT
→ FET operation depends only on the flow of majority carriers. Therefore they are called 'Unipolar Devices'.	→ In BJT, operation depends on both minority and majority Current Carriers. So BJT is a 'Bipolar Device'.
→ As FET has no junctions and the conduction is through an N-type or p-type Semiconducting material so FET is less noisy	→ More noisy
→ FET offers high input impedance and lower o/p impedance.	→ BJT offers high out-put impedance and lower input impedance.
→ It acts as an excellent Buffer amplifier	
→ It acts as a voltage Controlled device.	→ It acts as a Current Controlled device.
→ FETs are easier to fabricate. because of occupying less space it is suitable for IC's.	→ It occupies more space so we do not prefer more for ICs.
→ It has higher switching speeds and cut off frequencies	→ BJT Suffers lower switching speed and cut off frequencies.
→ Costlier to produce	→ cheaper to produce.
→ It has low gain Bandwidth product due to the junction Capacitive effects and produce more signal distortion except for Small signal operation.	→ It has Constant gain Bandwidth product.

Comparison between Depletion MOSFET and Enhancement MOSFET:-

Depletion MOSFET	Enhancement MOSFET
→ There is pse-existing channel.	→ There is no pse-existing channel and channel has to be created by applying pseper Gate to source voltage.
→ channel is diffused channel	→ channel is induced channel.
→ Suitable to operate both in the depletion mode and Enhancement mode.	→ Suitable to operate only in the enhancement mode.
→ Comparatively larger threshold voltage	→ Comparatively V_T is very small.
→ There is no channel length Modulation	→ channel length modulation exists.
→ when $V_{GS}=0$, I_D flows and is equal to I_{DSS}.	→ when V_{GS} is kept zero, there is no channel hence I_D is zero.

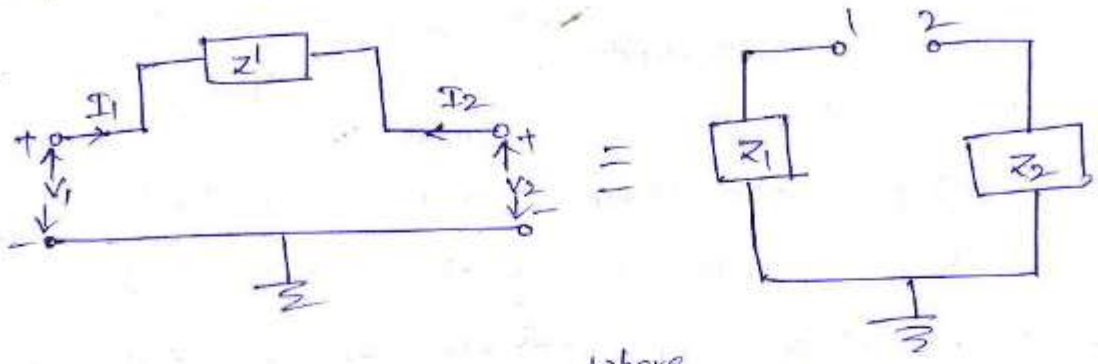
channel length Modulation:- when V_{DS} is applied, the length of the channel decreases. The process where the length of the channel changes by changing V_{DS} is called the 'channel length Modulation".

Comparison between JFET and MOSFET:-

JFET	MOSFET
→ Input impedance is smaller	→ Input impedance is larger.
→ power dissipation is more	→ power dissipation is less
→ More noisy.	→ Less noisy because of substrate is grounded.
→ Larger in size.	→ Smaller in size.
→ fabrication is complex	→ fabrication is easy.
→ JFET's are slower	→ MOSFET's are faster.
→ JFET is always operated mode depletion mode.	→ MOSFET's are operated mode both the modes i.e, enhancement and depletion modes.

Miller's Theorem :—

It states that 'If a series impedance Z' is existing between input and output terminals of the network, it can be replaced by shunt impedance Z_1 in the input section and by shunt impedance Z_2 in the output section'.



where

$$Z_1 = \frac{Z'}{1-A_V} \quad \text{and} \quad Z_2 = \frac{Z' A_V}{A_V - 1}$$

(i) If $V_1 > V_2$:

then I_1 flows.

$$\therefore I_1 = \frac{V_1 - V_2}{Z'} = \frac{V_1}{Z'}\left[1 - \frac{V_2}{V_1}\right] = \frac{V_1}{Z'}\left[1 - A_V\right]$$

$$I_1 = \frac{V_1}{Z'/[1-A_V]}$$

Since $I_1 = \frac{V_1}{Z_1}$

$$\therefore \boxed{Z_1 = \frac{Z'}{1-A_V}}$$

(ii) If $V_2 > V_1$: then I_2 flows.

$$\therefore I_2 = \frac{V_2 - V_1}{Z'} = \frac{V_2}{Z'}\left[1 - \frac{V_1}{V_2}\right]$$

$$I_2 = \frac{V_2}{Z'}\left[1 - \tfrac{1}{A_V}\right] = \frac{V_2}{Z'/\left[1 - \tfrac{1}{A_V}\right]}$$

Since $I_2 = \frac{V_2}{Z_2}$

$$\therefore \boxed{Z_2 = \frac{Z'}{1 - \frac{1}{A_V}} = \frac{Z' A_V}{A_V - 1}}$$